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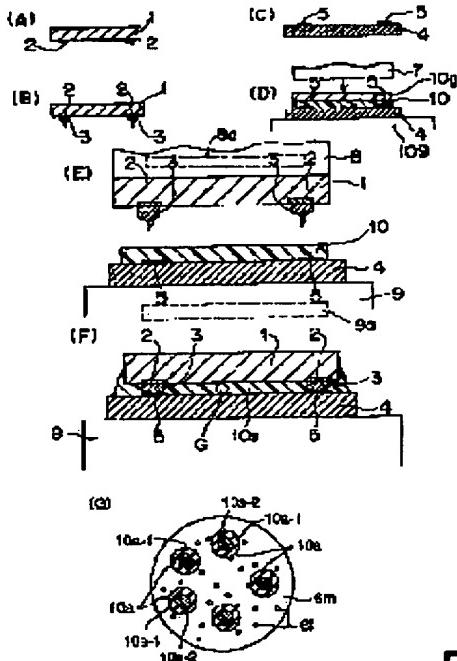
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(54) METHOD FOR MOUNTING ELECTRONIC COMPONENT AND DEVICE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an electronic component mounting method for jointing an electronic component to a board with good productivity and high reliability by means of arranging an anisotropic conduction layer having conducting particles, without the need for a sealing resin process or a bump leveling process.

SOLUTION: In a mounting method, bumps 3 and board electrodes 5 are positioned by interposing an anisotropic conduction layer 10, containing conduction particles 10a and inorganic fillers 6f in insulating resin. A chip 1 is pressurized to a board 4 by a head 8 with the welding pressure of not less than 20 gf per bump. Warpage of the chip and the board is corrected and insulating resin is cured, while the bumps are crushed so as to joint the chip and the board.



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CLAIMS

[Claim(s)]

[Claim 1] A ball (96 96a) is formed at the tip of a metal wire (95) by the electric spark like wirebonding. Carry out ultrasonic thermocompression bonding of the ball by which formation was carried out [above-mentioned] to the electrode (2) of electronic parts (1) by the capillary tube (93,193), and a bump (3,103) is formed. Making the anisotropy conductive layer (10) which blended the electric conduction particle (10a) with the insulating resin which blended the inorganic filler intervene Carrying out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the electrode (5) of the circuit board (4), carrying the above-mentioned electronic parts in the above-mentioned substrate, and heating from the above-mentioned electronic-parts side after that Or, heating from both by the side of the above-mentioned electronic parts and the above-mentioned substrate [while heating from a substrate side, or] Pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board, and crushing correction and the above-mentioned bump of the curvature of the above-mentioned substrate with a tool (8) The mounting approach of the electronic parts characterized by hardening the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board, joining the above-mentioned circuit board to the above-mentioned electronic parts, and connecting electrically the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board.

[Claim 2] The mounting approach of the electronic parts according to claim 1 prepared in the tip so that the bump by whom formation was done [above-mentioned] might be once pressed by the load of 20 or less gves and **** of the above-mentioned bump's neck part might be prevented, before carrying out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode (5) of the above-mentioned circuit board (4) and carrying the above-mentioned electronic parts in the above-mentioned substrate, making the above-mentioned anisotropy conductive layer intervene, after forming the above-mentioned bump.

[Claim 3] The amount of the above-mentioned inorganic filler which the above-mentioned insulating resin (6m) of the above-mentioned anisotropy conductive layer is an insulating thermosetting epoxy resin, and is blended with this insulating thermosetting epoxy resin is the mounting approach of the electronic parts according to claim 1 or 2 which are 5 - 90wt% of the above-mentioned insulating thermosetting epoxy resins.

[Claim 4] By stiffening the liquid of the insulating resin by which it was a liquid in case the above-mentioned insulating resin (6m) of the above-mentioned anisotropy conductive layer was applied to the above-mentioned substrate at the beginning, put in the above-mentioned substrate in the furnace (503), and spreading was carried out [above-mentioned] after applying to the above-mentioned substrate Or the mounting approach of electronic parts according to claim 1 to 3 of carrying the above-mentioned electronic parts in the above-mentioned substrate after semisolid-izing by pressing the liquid of the insulating resin by which spreading was carried out [above-mentioned] with the heated tool (78).

[Claim 5] A ball (96 96a) is formed at the tip of a metal wire (95) by the electric spark like wirebonding. Carry out ultrasonic thermocompression bonding of the ball by which formation was carried out [above-mentioned] to the electrode (2) of electronic parts (1) by the capillary tube (93,193), and a golden bump (3,103) is formed. Making the anisotropy conductive layer (10) which blended the electric conduction particle (10a) with the insulating resin which blended the inorganic filler intervene without leveling the bump by whom formation was done [above-mentioned] Carry out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the electrode (5) of the circuit board (4), and the

above-mentioned electronic parts are carried in the above-mentioned substrate. Then, while preparing a tip so that a load may be impressed from the top-face side of the above-mentioned electronic parts with a tool (8) and **** of the above-mentioned golden bump's neck part may be prevented, impress a supersonic wave and metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate is carried out. Next, heating from the above-mentioned top-face side of the above-mentioned electronic parts Or, heating from both by the side of the above-mentioned electronic parts and the above-mentioned substrate [while heating from the above-mentioned substrate side, or] Pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board, and crushing correction and the above-mentioned bump of the curvature of the above-mentioned substrate The mounting approach of the electronic parts characterized by hardening the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board, joining the above-mentioned circuit board to the above-mentioned electronic parts, and connecting electrically the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board.

[Claim 6] The above-mentioned electronic parts (1) have two or more electrodes (2). To the above-mentioned circuit board (4) in front of the above-mentioned alignment as the above-mentioned anisotropy conductive layer After sticking the solid anisotropy electric conduction film sheet (10) of a geometry smaller than the dimension (OL) which tied two or more above-mentioned electrodes (2) of the above-mentioned electronic parts (1), the above-mentioned alignment is performed. In the above-mentioned junction, heating the above-mentioned anisotropy electric conduction film sheet (10) Carrying out the pressurization press of the above-mentioned electronic parts at the above-mentioned circuit board, and correcting the curvature of the above-mentioned circuit board to coincidence The mounting approach of the electronic parts according to claim 1 to 5 which harden the above-mentioned insulating resin which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board, and joined the above-mentioned circuit board to the above-mentioned electronic parts.

[Claim 7] When forming a golden ball (96a) at the tip of a metal wire (95) by the electric spark like [in case the above-mentioned bump is formed on the above-mentioned electronic parts] wirebonding. By the above-mentioned capillary tube which has the tip configuration which does not establish an even part in the part which makes a chamfer angle (thetac) 100 degrees or less, and touches the above-mentioned golden ball The mounting approach of electronic parts according to claim 1 to 6 that a tip forms the profile conic above-mentioned golden bump in the above-mentioned electrode of the above-mentioned electronic parts.

[Claim 8] A ball (96 96a) is formed at the tip of a metal wire (95) by the electric spark like wirebonding. A bump (3,103) is formed in the electrode (2) of electronic parts (1) for the ball by which formation was carried out [above-mentioned] by the capillary tube (93,193). Making the anisotropy conductive layer (10) which blended the electric conduction particle (10a) with the insulating resin which blended the inorganic filler intervene without leveling the bump by whom formation was done [above-mentioned] Carry out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the electrode (5) of the circuit board (4), carry the above-mentioned electronic parts in the above-mentioned substrate, and after that, heating from the top face of the above-mentioned electronic parts with the tool (8) heated by predetermined temperature Pressing the above-mentioned electronic parts with a pressure P1 to the above-mentioned circuit board as welding pressure, and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. Then, dropping the above-mentioned welding pressure to the pressure P2 lower than the above-mentioned pressure P1, and easing the stress at the time of hardening of the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer after predetermined time The mounting approach of the electronic parts characterized by joining the above-mentioned circuit board to the above-mentioned electronic parts, and connecting electrically the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board.

[Claim 9] For the above-mentioned pressure P2, the above-mentioned pressure P1 is the mounting approach of the electronic parts according to claim 8 made or less [of the above-mentioned pressure P1] into 1/2 more than 20gf(s) / bump.

[Claim 10] The equipment which sticks on the electrode (5) or electronic parts (1) of the circuit board (4) the anisotropy conductive layer (10) which blended the electric conduction particle (10a) with the insulating resin which blended the inorganic filler (7,109,200,201), A ball (96 96a) is formed at the tip of a metal wire

(95) by the electric spark like [the electrode (2) of the above-mentioned electronic parts (1)] wirebonding. The equipment which forms the bump (3,103) who does ultrasonic thermocompression bonding of this to the above-mentioned electrode of the above-mentioned substrate by the capillary tube (93,193), forms it, and does not level it (93,193), With the equipment (600) which carries out alignment of the above-mentioned electronic parts to the above-mentioned electrode (5) of the above-mentioned circuit board (4), and carries them, and a tool (8) Pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board, heating, and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. Mounting equipment of the electronic parts characterized by having equipment (8 9) which joins the above-mentioned circuit board to the above-mentioned electronic parts, and connects electrically the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board.

[Claim 11] The amount of the above-mentioned inorganic filler which the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer is an insulating thermosetting epoxy resin, and is blended with this insulating thermosetting epoxy resin is mounting equipment of the electronic parts according to claim 10 which are 5 - 90wt% of the above-mentioned insulating thermosetting epoxy resins.

[Claim 12] The above-mentioned insulating resin (6 m) of the above-mentioned anisotropy conductive layer is mounting equipment of electronic parts [equipped with the furnace (503) which is made to insert and harden the substrate by which spreading was carried out / above-mentioned / in the liquid of the above-mentioned insulating resin which is a liquid and was applied to the above-mentioned substrate by the dispenser (502) which applies the liquid of the above-mentioned insulating resin to the above-mentioned substrate, and this dispenser, and semisolid-izes the above-mentioned insulating resin] according to claim 10 or 11.

[Claim 13] The above-mentioned insulating resin (6m) of the above-mentioned anisotropy conductive layer is mounting equipment of electronic parts [equipped with the equipment (78) which presses the liquid of the above-mentioned insulating resin which is a liquid and was applied to the above-mentioned substrate by the dispenser (502) which applies the liquid of the above-mentioned insulating resin to the above-mentioned substrate, and this dispenser, and semisolid-izes the above-mentioned insulating resin] according to claim 10 or 11.

[Claim 14] The equipment which sticks on the electrode (5) or electronic parts (1) of the circuit board (4) the anisotropy conductive layer (10) which blended the electric conduction particle (10a) with the insulating resin which blended the inorganic filler (7,109,200,201), A ball (96 96a) is formed at the tip of a metal wire (95) by the electric spark like [the electrode (2) of the above-mentioned electronic parts (1)] wirebonding. The equipment which forms the golden bump (3,103) who does ultrasonic thermocompression bonding of this to the above-mentioned electrode of the above-mentioned substrate by the capillary tube (93,193), forms it, and does not level it (93,193), The equipment which carries out alignment of the above-mentioned electronic parts to the above-mentioned electrode (5) of the above-mentioned circuit board (4), and carries them (600), Impressing a supersonic wave and heating the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate with the equipment (620) which carries out metal junction, and a tool (8), while preparing a tip so that a load may be impressed from the top face of the above-mentioned electronic parts with a tool (628) and **** of the above-mentioned golden bump's neck part may be prevented Crushing the above-mentioned bump, while pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. Mounting equipment of the electronic parts characterized by having equipment (8 9) which joins the above-mentioned circuit board to the above-mentioned electronic parts, and connects electrically the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board.

[Claim 15] In front of the above-mentioned alignment, to the above-mentioned circuit board (4), as the above-mentioned anisotropy conductive layer The equipment which sticks the solid anisotropy electric conduction film sheet (10) of a geometry smaller than the dimension (OL) which tied the electrode (2) of the above-mentioned electronic parts (1) (640), Then, it sets to the equipment (600) which equips by performing alignment of the above-mentioned circuit board and electronic parts, and junction. The pressurization press of the above-mentioned electronic parts is carried out at the above-mentioned circuit board, heating the

above-mentioned anisotropy electric conduction film sheet (10). Mounting equipment of the electronic parts possessing the equipment (7 8) which hardens the above-mentioned anisotropy electric conduction film sheet which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board, and joins the above-mentioned circuit board to the above-mentioned electronic parts while correcting the curvature of the above-mentioned circuit board to coincidence according to claim 10 to 13.

[Claim 16] The equipment (93,193) which forms the above-mentioned golden ball (96a) is mounting equipment of the electronic parts according to claim 10 to 15 with which it has the above-mentioned capillary tube from which a chamfer angle (thetac) becomes 100 degrees or less while having the tip configuration which does not establish an even part in the part which touches the above-mentioned golden ball, and a tip forms the profile conic above-mentioned golden bump in the above-mentioned electrode of the above-mentioned electronic parts by this capillary tube.

[Claim 17] The equipment which sticks on the circuit board (4) or electronic parts (1) the anisotropy conductive layer (10) which blended the electric conduction particle (10a) with the insulating resin which blended the inorganic filler (7,109,200,201), A ball (96 96a) is formed at the tip of a metal wire (95) by the electric spark like [the electrode (2) of the above-mentioned electronic parts (1)] wirebonding. The equipment which forms the bump (3,103) who forms this in the above-mentioned electrode of the above-mentioned substrate by the capillary tube (93,193), and does not level it (93,193), With the equipment (600) which carries out alignment of the above-mentioned electronic parts to the above-mentioned electrode (5) of the above-mentioned circuit board (4), and carries them, and the tool (8) heated by predetermined temperature Pressing the above-mentioned electronic parts with a pressure P1 to the above-mentioned circuit board as welding pressure, heating from the top face of the above-mentioned electronic parts, and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. Then, predetermined time of after, Dropping the above-mentioned welding pressure to the pressure P2 lower than the above-mentioned pressure P1, and easing the stress at the time of hardening of the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer Mounting equipment of the electronic parts characterized by having equipment (8 9) which joins the above-mentioned circuit board to the above-mentioned electronic parts, and connects electrically the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board.

[Claim 18] For the above-mentioned pressure P2, the above-mentioned pressure P1 is mounting equipment of the electronic parts according to claim 17 made or less [of the above-mentioned pressure P1] into 1/2 more than 20gf(s) / bump.

[Claim 19] The mounting approach of the electronic parts according to claim 1 to 3 characterized by the mean particle diameter of the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer being 3 micrometers or more.

[Claim 20] claim 1- which is two or more kinds of inorganic fillers (6f-1, 6f-2) with the mean particle diameter from which the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer differs -- the mounting approach of electronic parts given in 3 or 19.

[Claim 21] The above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer They are at least two kinds of inorganic fillers (6f-1, 6f-2) with the mean particle diameter from which plurality differs. the above -- the mean particle diameter of one inorganic filler of two kinds of inorganic fillers (6f-1), even if few the above -- claim 1- from which the mean particle diameter of the inorganic filler (6f-2) of another side of two kinds of inorganic fillers differs more than twice even if few -- the mounting approach of electronic parts given in 3 or 19.

[Claim 22] The above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer They are at least two kinds of inorganic fillers (6f-1, 6f-2) with the mean particle diameter from which plurality differs. Even if few, one inorganic filler of two kinds of inorganic fillers (6f-1) has the mean particle diameter exceeding 3 micrometers. the above -- the above -- claim 1- in which the inorganic filler (6f-2) of another side of two kinds of inorganic fillers has the mean particle diameter of 3 micrometers or less even if few -- the mounting approach of electronic parts given in 3 or 19.

[Claim 23] The above-mentioned inorganic filler (6f) blended with the above-mentioned insulating resin (6m) of the above-mentioned anisotropy conductive layer They are at least two kinds of inorganic fillers (6f-1, 6f-2) with the mean particle diameter from which plurality differs. the above -- claim 1- which the mean particle diameter of two kinds of inorganic fillers is large, and does a stress relaxation operation so when an

inorganic filler (6f-1) consists of the same ingredient as the above-mentioned insulating resin even if few -- the mounting approach of electronic parts given in 3 or 19.

[Claim 24] The above-mentioned inorganic filler (6f) blended with the above-mentioned insulating resin (6m) of the above-mentioned anisotropy conductive layer They are at least two kinds of inorganic fillers (6f-1, 6f-2) with the mean particle diameter from which plurality differs. Softer than the epoxy resin of the mean particle diameter of two kinds of inorganic fillers whose inorganic filler (6f-1) while is large and is the above-mentioned insulating resin (6m), even if few the above -- claim 1- which does a stress relaxation operation so by compressing the inorganic filler (6f-1) of the method of top Norikazu -- the mounting approach of electronic parts given in 3 or 19.

[Claim 25] For the above-mentioned anisotropy conductive layer, the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate is the mounting approach of electronic parts given in either [claims 1-3 it was made to have few above-mentioned amounts of inorganic fillers than other parts, and] 19-24.

[Claim 26] The above-mentioned anisotropy conductive layer is the mounting approach of electronic parts [equipped with the 2nd resin layer (6y) which contacts the 1st resin layer (6x) which was located in the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and blended the above-mentioned inorganic filler with the same insulating resin as the above-mentioned insulating resin, and the above-mentioned 1st resin layer, and consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 1st resin layer] according to claim 25.

[Claim 27] For the above-mentioned anisotropy conductive layer, the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively is the mounting approach of electronic parts according to claim 25 it was made to have few above-mentioned amounts of inorganic fillers than other parts.

[Claim 28] The above-mentioned 2nd resin layer of the above-mentioned 1st resin layer is the mounting approach of electronic parts according to claim 26 that have further the 3rd resin layer (6z) from which the above-mentioned anisotropy conductive layer is constituted from insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 1st resin layer by the opposite side, and the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer contact the above-mentioned electronic parts and the above-mentioned substrate, respectively.

[Claim 29] It is the mounting approach of electronic parts according to claim 27 that the above-mentioned amount of inorganic fillers of a part besides the above is more than 20wt% while the above-mentioned amount of inorganic fillers makes less than [20wt%] the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively.

[Claim 30] It is the mounting approach of electronic parts according to claim 28 that the above-mentioned amount of inorganic fillers of the above-mentioned 2nd resin layer is more than 20wt% while the above-mentioned amount of inorganic fillers makes each of the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer less than [20wt%].

[Claim 31] The above-mentioned anisotropy conductive layer is the mounting approach of electronic parts given in either [claims 1-3 made it whose above-mentioned amounts of inorganic fillers decrease gradually or gradually toward other parts from the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and] 19-24.

[Claim 32] The above-mentioned anisotropy conductive layer is the mounting approach of the electronic parts according to claim 31 made it whose above-mentioned amount of inorganic fillers decrease gradually or gradually toward other parts from the part which contacts, respectively in the above-mentioned electronic parts and the above-mentioned substrate.

[Claim 33] The mounting approach of electronic parts given in either of claims 25, 27, 29, and 31 which used the insulating resin which raises adhesion to the ingredient on the front face of a substrate in the part in contact with the above-mentioned substrate while using the insulating resin which raises adhesion to the film material used for an electronic-parts front face in the part in contact with the above-mentioned electronic parts.

[Claim 34] The mounting approach of electronic parts given in either of claims 26, 28, 30, and 32 which used the insulating resin which raises adhesion to the ingredient on the front face of a substrate in the above-mentioned resin layer in contact with the above-mentioned substrate while using the insulating resin which raises adhesion to the film material used for an electronic-parts front face in the above-mentioned resin layer in contact with the above-mentioned electronic parts.

[Claim 35] The above-mentioned anisotropy conductive layer (10) is the mounting approach of electronic

parts given in either [claims 1-3 with which it was made for the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate not to blend the above-mentioned inorganic filler, and] 19-24.

[Claim 36] The above-mentioned anisotropy conductive layer (10) is the mounting approach of electronic parts [equipped with the 2nd resin layer (6y) which consists of insulating resin which contacts the 1st resin layer (6x) which was located in the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and blended the above-mentioned inorganic filler with the same insulating resin as the above-mentioned insulating resin, and the above-mentioned 1st resin layer, and does not blend the above-mentioned inorganic filler] according to claim 35.

[Claim 37] The above-mentioned anisotropy conductive layer (10) is the mounting approach of electronic parts according to claim 35 of having made it the part which contacts, respectively not blend the above-mentioned inorganic filler with the above-mentioned electronic parts and the above-mentioned substrate.

[Claim 38] For the above-mentioned 2nd resin layer of the above-mentioned 1st resin layer, the above-mentioned anisotropy conductive layer (10) is the mounting approach of electronic parts according to claim 36 that have further the 3rd resin layer (6z) which consists of insulating resin which does not blend the above-mentioned inorganic filler with the opposite side, and the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer contact the above-mentioned electronic parts and the above-mentioned substrate, respectively.

[Claim 39] It is the mounting approach of electronic parts according to claim 37 that the above-mentioned amount of inorganic fillers of a part besides the above is more than 20wt% while making it the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively not blend the above-mentioned inorganic filler.

[Claim 40] It is the mounting approach of electronic parts according to claim 38 that the above-mentioned amount of inorganic fillers of the above-mentioned 2nd resin layer is more than 20wt% while making it each of the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer not blend the above-mentioned inorganic filler.

[Claim 41] The 4th resin layer which consists of insulating resin which the above-mentioned anisotropy conductive layer (10) was located in the part in contact with the above-mentioned electronic parts and the above-mentioned substrate, and blended the above-mentioned inorganic filler (6v), Claims 1-3 equipped with the 5th resin layer (6w) which is located in the interstitial segment of the above-mentioned electronic parts and the above-mentioned substrate, and consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 4th resin layer, the mounting approach of electronic parts given in either 19-24.

[Claim 42] The 4th resin layer which consists of insulating resin which the above-mentioned anisotropy conductive layer (10) was located in the part in contact with the above-mentioned electronic parts and the above-mentioned substrate, and blended the above-mentioned inorganic filler (6v), Claims 1-3 equipped with the 5th resin layer (6w) which consists of insulating resin by which it is located in the interstitial segment of the above-mentioned electronic parts and the above-mentioned substrate, and the above-mentioned amount of inorganic fillers is not contained, the mounting approach of electronic parts given in either 19-24.

[Claim 43] The above-mentioned anisotropy conductive layer (10) is the mounting approach of electronic parts given in either [claims 1-3 made it whose above-mentioned amounts of inorganic fillers decrease gradually from the part which contacts, respectively toward an interstitial segment with the above-mentioned electronic parts and the above-mentioned substrate in the above-mentioned electronic parts and the above-mentioned substrate, and] 19-24.

[Claim 44] the above-mentioned anisotropy conductive layer (10) -- the near part of the above-mentioned electronic parts -- subsequently -- the near part of the above-mentioned substrate -- subsequently -- the order of the interstitial segment of the near part of the above-mentioned electronic parts, and the near part of the above-mentioned substrate -- the above-mentioned amount of inorganic fillers -- few -- having made -- the mounting approach of electronic parts given in either [claims 1-3 and] 19-24.

[Claim 45] Each amount of inorganic fillers of the near part of the above-mentioned electronic parts of the above-mentioned anisotropy conductive layer (10) and the near part of the above-mentioned substrate is the mounting approach of the electronic parts according to claim 43 or 44 blended respectively corresponding to the coefficient of linear expansion of the part in contact with the above-mentioned anisotropy conductive layer of the coefficient of linear expansion of a part, and the above-mentioned substrate in contact with the above-mentioned anisotropy conductive layer of the above-mentioned electronic parts.

[Claim 46] Where it made the anisotropy conductive layer (10) which the bump (3,103) formed in the electrode (2) of electronic parts (1) was blended in the inorganic filler (6f) at insulating resin (6m), and was hardened in her intervene and the above-mentioned bump is crushed It was joined to the electrode (5) of the circuit board (4), and the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board are connected electrically. The above-mentioned anisotropy conductive layer (10) The electronic-parts unit to which the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate is characterized by making it there be few above-mentioned amounts of inorganic fillers than other parts.

[Claim 47] Where it made the anisotropy conductive layer (10) which the bump (3,103) formed in the electrode (2) of electronic parts (1) was blended in the inorganic filler (6f) at insulating resin (6m), and was hardened in her intervene and the above-mentioned bump is crushed It was joined to the electrode (5) of the circuit board (4), and the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board are connected electrically. The above-mentioned anisotropy conductive layer (10) The 1st resin layer which was located in the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and blended the above-mentioned inorganic filler with the same insulating resin as the above-mentioned insulating resin (6x), The electronic-parts unit characterized by having the 2nd resin layer (6y) which contacts the above-mentioned 1st resin layer, and consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 1st resin layer.

[Claim 48] The mounting approach of the electronic parts according to claim 5 heated from both by the side of the above-mentioned electronic parts and the above-mentioned substrate when impressing the above-mentioned supersonic wave and carrying out metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate while heating from the above-mentioned top-face side of the above-mentioned electronic parts, or while heating from the above-mentioned substrate side.

[Claim 49] claims 1-9 and 19- the electronic-parts unit by which the above-mentioned electronic parts were mounted in the above-mentioned substrate by the mounting approach of electronic parts given in 45 or 48.

[Claim 50] The above-mentioned bump is the mounting approach of electronic parts given in either [claims 1-9 which are the bumps who formed by plating or printing, and] 19-45.

[Claim 51] The above-mentioned bump is an electronic-parts unit according to claim 46 to 49 which is the bump who formed by plating or printing.

[Claim 52] claims 1-9 which blended the electric conduction particle (10a) which has a larger average diameter than the mean particle diameter of the above-mentioned inorganic filler with the solid insulating resin with which the above-mentioned anisotropy conductive layer blended the above-mentioned inorganic filler, and 19- the mounting approach of electronic parts given in 45 or 50.

[Claim 53] The above-mentioned anisotropy conductive layer is mounting equipment of the electronic parts according to claim 10 to 18 with which the mean particle diameter of the above-mentioned inorganic filler blended the electric conduction particle (10a) which has a larger average diameter with the solid insulating resin which blended the above-mentioned inorganic filler (6f).

[Claim 54] claim 46- by which the mean particle diameter of the above-mentioned inorganic filler blended the electric conduction particle (10a) which has a larger average diameter with the solid insulating resin with which the above-mentioned anisotropy conductive layer blended the above-mentioned inorganic filler (6f) -- an electronic-parts unit given in 49 or 51.

[Claim 55] The equipment which impresses the above-mentioned supersonic wave and carries out metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate is mounting equipment of the electronic parts according to claim 14 which are equipped with the heating component heated from both by the side of the above-mentioned electronic parts and the above-mentioned substrate from the above-mentioned substrate side, and were heated by the above-mentioned heating component at the time of the above-mentioned metal junction from the above-mentioned top-face side of the above-mentioned electronic parts.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention is a printed circuit board for electronic circuitries (on these specifications, although a "substrate" is called as an example of representation). in this "substrate", covering arrival objects, such as other components with which it is equipped with INTAPOZA or electronic parts, are meant. By the mounting approach, its equipment, and the above-mentioned mounting approach of electronic parts to the circuit board which mounts electronic parts, for example, IC chip, a surface-acoustic-waves (SAW) device, etc., in the state of a simple substance (the case of IC chip raise in basic wages IC) The above-mentioned electronic parts are related with the electronic-parts unit mounted in the above-mentioned substrate.

[0002]

[Description of the Prior Art] A today and electronic-circuitry substrate comes to be used for all products, the engine performance improves day by day, and flip chip mounting to which it is high and an impedance becomes low serves as the mounting approach suitable for the electronic equipment by which the frequency used on the circuit board also uses a RF. Moreover, flip chip mounting which carries IC chip in the circuit board with the nakedness instead of a package is called for from the increment in a pocket device. for this reason, IC chip -- it remains as it is -- a fixed number of defectives are intermingled for IC chip when carrying in the circuit board alone, and IC chip mounted to electronic equipment and flat panel DISUBUREI. Moreover, CSP (Chip SizePackage), BGA (Ball Grid Array), etc. are increasingly used besides the above-mentioned flip chip.

[0003] There are some which were indicated by JP,06-66355,B etc. as an approach (conventional example 1) of joining IC chip to the circuit board of the conventional electronic equipment. This is shown in drawing 15 R> 5. As shown in drawing 15, after imprinting the Ag paste 74 for the IC chip 71 in which the bump 73 was formed and connecting with the electrode 75 of the circuit board 76, the Ag paste 74 is hardened, and generally the approach of slushing a sealing agent 78 between the IC chip 71 and the circuit board 76 is learned after that.

[0004] moreover, like JP,62-6652,B shown in drawing 16 as an approach (conventional example 2) of joining IC chip to a liquid crystal display Use the anisotropy electric conduction film 80, remove the anisotropy electric conduction adhesives layer 81 which adds and constitutes the conductive mote 82 in insulating resin 83 from a separator 85, and it applies to the glass of a substrate or a liquid crystal display 84. Generally by carrying out thermocompression bonding of the IC chip 86, the connection structure of a semiconductor chip where the above-mentioned anisotropy electric conduction adhesives layer 81 intervenes between the inferior surface of tongue of IC chips 86 other than under the Au bump 87 and a substrate 84 is known.

[0005] As a conventional example 3, UV hardening resin is applied to a substrate, mounting and pressurizing IC chip on it, by carrying out UV irradiation, the resin between both is hardened and the method of maintaining contact between both according to the shrinkage force is learned.

[0006] Thus, in order to have joined IC chip, the above-mentioned junction was performed by carrying out die bonding of an IC chip like a flat package on a leadframe, carrying out wire bond of the electrode and leadframe of IC chip, printing a cream pewter to the circuit board and performing the process of carrying a flat package IC and carrying out a reflow on it, after carrying out resin shaping and forming a package, a bond and. The process which makes IC a package by the method of construction called such SMT (Surface Mount Technology) was long, and it was difficult for production of IC components to take time amount, and to miniaturize the circuit board. For example, where the closure is carried out to a flat pack, since IC chip

needed about about 4 to 10 times [of IC chip] area, it had become the factor which bars a miniaturization. [0007] On the other hand, recently, the flip chip method of construction which carries IC chip in a substrate direct in the state of nakedness for compaction of a process and the formation of small lightweight has come to be used. This flip chip method of construction performs in parallel bump formation for IC chip, bump leveling, an Ag-Pd paste imprint, mounting, inspection, the closure by closure resin, stud bump bonding (SBB) that conducts inspection, and bump formation for IC chip and UV hardening resin spreading to a substrate, and the method of construction of many like UV resin junction which conduct mounting, UV hardening of resin, and inspection is developed after that.

[0008]

[Problem(s) to be Solved by the Invention] However, hardening of a paste and spreading hardening of closure resin which join the bump of IC chip and the electrode of a substrate in every method of construction took time amount, and it had the fault that productivity was bad. Moreover, there was the need of using the ceramic and glass which had the amount of curvatures managed as the circuit board, and it had the fault which becomes expensive.

[0009] Moreover, in the method of construction which uses a conductive paste like the conventional example 1 for a jointing material for corrugated fibreboard, in order to stabilize the amount of imprints, the bump of IC chip leveled, and after she did flattening, she needed to use.

[0010] Moreover, in the junction structure by anisotropy electric conduction adhesives like the conventional example 2, although the thing using glass as a base material of the circuit board is developed Although it is necessary to distribute the electric conduction particle in electroconductive glue to homogeneity since it is necessary to put an electric conduction particle between two electrodes for the electric flow between IC tip side electrode and a substrate lateral electrode It was difficult to distribute the electric conduction particle in electroconductive glue to homogeneity, and it had to become a short cause by the distributed abnormalities of a particle, or electroconductive glue had to be expensive, and in order to arrange a bump's height, the bump of the electrode of IC chip had to form by electroplating.

[0011] Moreover, in the approach of joining using UV hardening resin like the conventional example 3, a bump's height variation had to be made below into **one (micrometer), and there was a problem of being unjoinable in a substrate with the bad flatness of a resin substrate (glass epoxy group plate) etc. Moreover, also in the approach using a pewter, in order to ease the thermal-expansion differential shrinkage of a substrate and IC chip after junction, closure resin needed to be slushed and hardened. 2 - 8-hour time amount was needed for hardening of this resin seal, and there was a problem that productivity was very bad in it.

[0012] Therefore, after the purpose of this invention being to solve the above-mentioned problem and joining electronic parts to the circuit board The bump leveling process of arranging uniformly the height of the closure resin process slushed between electronic parts and a substrate or a bump is not needed. The anisotropy conductive layer which has an electric conduction particle is made to intervene, and it is in offering the electronic-parts unit by which the above-mentioned electronic parts were mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of electronic parts to the circuit board which joins electronic parts with productivity sufficient to a substrate with high-reliability.

[0013]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is constituted as follows.

[0014] If this invention is caused like the 1st voice, a ball will be formed at the tip of a metal wire by the electric spark like wirebonding. Making the anisotropy conductive layer which blended the electric conduction particle with the insulating resin which carried out ultrasonic thermocompression bonding of the ball by which formation was carried out [above-mentioned] to the electrode of electronic parts by the capillary tube, formed the bump, and blended the inorganic filler intervene Heating from a substrate side [while alignment of the above-mentioned electrode of the above-mentioned electronic parts and the electrode of the circuit board is carried out, and the above-mentioned electronic parts are carried in the above-mentioned substrate and heating from the above-mentioned electronic-parts side after that, or] Or, pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board by the tool, heating from both by the side of the above-mentioned electronic parts and the above-mentioned substrate, and crushing correction and the above-mentioned bump of the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and

the above-mentioned circuit board is hardened, and the mounting approach of the electronic parts characterized by joining the above-mentioned circuit board to the above-mentioned electronic parts, and connecting electrically the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board is offered.

[0015] Making the above-mentioned anisotropy conductive layer intervene, after forming the above-mentioned bump, if this invention is caused like the 2nd voice Before carrying out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the above-mentioned electrode of the above-mentioned circuit board and carrying the above-mentioned electronic parts in the above-mentioned substrate The mounting approach of the electronic parts a publication is offered [having prepared the tip so that the bump by whom formation was done / above-mentioned / might be once pressed by the load of 20 or less gves and **** of the above-mentioned bump's neck part might be prevented] like the 1st voice.

[0016] the 1st whose amount of the above-mentioned inorganic filler blended with this insulating thermosetting epoxy resin the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer will be an insulating thermosetting epoxy resin, and will be 5 - 90wt% of the above-mentioned insulating thermosetting epoxy resin if this invention is caused like the 3rd voice -- or the mounting approach of the electronic parts a publication is offered like 2 voice.

[0017] By stiffening the liquid of the insulating resin by which it was a liquid in case the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer was applied to the above-mentioned substrate at the beginning, put in the above-mentioned substrate in the furnace and spreading was carried out [above-mentioned] after applying to the above-mentioned substrate, if this invention is caused like the 4th voice Or after semisolid-izing by pressing the liquid of the insulating resin by which spreading was carried out [above-mentioned] with the heated tool, the 1-3rd ones which carry the above-mentioned electronic parts in the above-mentioned substrate of modes is provided with the mounting approach of the electronic parts a publication.

[0018] If this invention is caused like the 5th voice, a ball will be formed at the tip of a metal wire by the electric spark like wirebonding. Carry out ultrasonic thermocompression bonding of the ball by which formation was carried out [above-mentioned] to the electrode of electronic parts by the capillary tube, and a golden bump is formed. Making the anisotropy conductive layer which blended the electric conduction particle with the insulating resin which blended the inorganic filler intervene without leveling the bump by whom formation was done [above-mentioned] Carry out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the electrode of the circuit board, and the above-mentioned electronic parts are carried in the above-mentioned substrate. Then, while preparing a tip so that a load may be impressed from the top-face side of the above-mentioned electronic parts with a tool and **** of the above-mentioned golden bump's neck part may be prevented, impress a supersonic wave and metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate is carried out. Next, heating from the above-mentioned top-face side of the above-mentioned electronic parts Or, heating from both by the side of the above-mentioned electronic parts and the above-mentioned substrate [while heating from the above-mentioned substrate side, or] Pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board, and crushing correction and the above-mentioned bump of the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened, and the mounting approach of the electronic parts characterized by joining the above-mentioned circuit board to the above-mentioned electronic parts, and connecting electrically the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board is offered.

[0019] If this invention is caused like the 6th voice, the above-mentioned electronic parts have two or more electrodes. To the above-mentioned circuit board in front of the above-mentioned alignment as the above-mentioned anisotropy conductive layer After sticking the solid anisotropy electric conduction film sheet of a geometry smaller than the dimension which tied two or more above-mentioned electrodes of the above-mentioned electronic parts, perform the above-mentioned alignment, and it sets to the above-mentioned junction. The pressurization press of the above-mentioned electronic parts is carried out at the above-mentioned circuit board, heating the above-mentioned anisotropy electric conduction film sheet. Correcting the curvature of the above-mentioned circuit board to coincidence, the above-mentioned insulating resin which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened, and the 1-5th ones which joined the above-mentioned circuit board to the above-mentioned

electronic parts of modes is provided with the mounting approach of the electronic parts a publication. [0020] When forming a golden ball at the tip of a metal wire by the electric spark like [if this invention is caused like the 7th voice / in case the above-mentioned bump is formed on the above-mentioned electronic parts] wirebonding, By the above-mentioned capillary tube which has the tip configuration which does not establish an even part in the part which makes a chamfer angle 100 degrees or less, and touches the above-mentioned golden ball The 1-6th ones by which a tip forms the profile conic above-mentioned golden bump in the above-mentioned electrode of the above-mentioned electronic parts of modes is provided with the mounting approach of the electronic parts a publication.

[0021] If this invention is caused like the 8th voice, a ball will be formed at the tip of a metal wire by the electric spark like wirebonding. Making the anisotropy conductive layer which blended the electric conduction particle with the insulating resin which blended the inorganic filler intervene without forming a bump in the electrode of electronic parts for the ball by which formation was carried out [above-mentioned] by the capillary tube, and leveling the bump by whom formation was done [above-mentioned] Carry out alignment of the above-mentioned electrode of the above-mentioned electronic parts, and the electrode of the circuit board, carry the above-mentioned electronic parts in the above-mentioned substrate, and after that, heating from the top face of the above-mentioned electronic parts with the tool heated by predetermined temperature Pressing the above-mentioned electronic parts with a pressure P1 to the above-mentioned circuit board as welding pressure, and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. Then, dropping the above-mentioned welding pressure to the pressure P2 lower than the above-mentioned pressure P1, and easing the stress at the time of hardening of the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer after predetermined time The mounting approach of the electronic parts characterized by joining the above-mentioned circuit board to the above-mentioned electronic parts, and connecting electrically the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board is offered.

[0022] if this invention is caused like the 9th voice, the above-mentioned pressure P1 will make the above-mentioned pressure P2 1/2 or less [of the above-mentioned pressure P1] more than 20gf(s) / bump -- the mounting approach of the electronic parts a publication is offered like the 8th voice.

[0023] The equipment which sticks on the electrode or electronic parts of the circuit board the anisotropy conductive layer which blended the electric conduction particle with the insulating resin which blended the inorganic filler when this invention was caused like the 10th voice, The equipment which forms a ball at the tip of a metal wire by the electric spark like [the electrode of the above-mentioned electronic parts] wirebonding, and forms the bump who does ultrasonic thermocompression bonding of this to the above-mentioned electrode of the above-mentioned substrate by the capillary tube, forms it, and does not level it, With the equipment which carries out alignment of the above-mentioned electronic parts to the above-mentioned electrode of the above-mentioned circuit board, and carries them, and a tool Pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board, heating, and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. The mounting equipment of the electronic parts characterized by having equipment which joins the above-mentioned circuit board to the above-mentioned electronic parts, and connects electrically the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board is offered.

[0024] if this invention is caused like the 11th voice, the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer will be an insulating thermosetting epoxy resin, and the amount of the above-mentioned inorganic filler blended with this insulating thermosetting epoxy resin will be 5 - 90wt% of the above-mentioned insulating thermosetting epoxy resin -- the mounting equipment of the electronic parts of a publication is offered like the 10th voice.

[0025] the 10th which the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer is a liquid, and it had in the furnace which make insert and harden the dispenser which applies the liquid of the above-mentioned insulating resin to the above-mentioned substrate, and the substrate by which spreading was carried out [above-mentioned] in the liquid of the above-mentioned insulating resin applied to the above-mentioned substrate by this dispenser, and semisolid-izes in the above-mentioned insulating resin when this invention was caused like the 12th voice -- or the mounting equipment of the electronic parts

of a publication provides like 11 voice.

[0026] the 10th which the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer is a liquid, and will be equipped with the dispenser which applies the liquid of the above-mentioned insulating resin to the above-mentioned substrate, and the equipment which presses the liquid of the above-mentioned insulating resin applied to the above-mentioned substrate by this dispenser, and semisolid-izes the above-mentioned insulating resin if this invention is caused like the 13th voice -- or the mounting equipment of the electronic parts of a publication offers like 11 voice.

[0027] The equipment which sticks on the electrode or electronic parts of the circuit board the anisotropy conductive layer which blended the electric conduction particle with the insulating resin which blended the inorganic filler when this invention was caused like the 14th voice, A ball is formed at the tip of a metal wire by the electric spark like [the electrode of the above-mentioned electronic parts] wirebonding. The equipment which forms the golden bump who does ultrasonic thermocompression bonding of this to the above-mentioned electrode of the above-mentioned substrate by the capillary tube, forms it, and does not level it, The equipment which carries out alignment of the above-mentioned electronic parts to the above-mentioned electrode of the above-mentioned circuit board, and carries them, The equipment which impresses a supersonic wave and carries out metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate while preparing a tip so that a load may be impressed from the top face of the above-mentioned electronic parts with a tool and **** of the above-mentioned golden bump's neck part may be prevented, Crushing the above-mentioned bump, while pressing the above-mentioned electronic parts with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board and correcting the curvature of the above-mentioned substrate, heating with a tool The above-mentioned insulating resin of the above-mentioned anisotropy conductive layer which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened. The mounting equipment of the electronic parts characterized by having equipment which joins the above-mentioned circuit board to the above-mentioned electronic parts, and connects electrically the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board is offered.

[0028] If this invention is caused like the 15th voice, to the above-mentioned circuit board in front of the above-mentioned alignment as the above-mentioned anisotropy conductive layer The equipment which sticks the solid anisotropy electric conduction film sheet of a geometry smaller than the dimension which tied the electrode of the above-mentioned electronic parts, Then, it sets to the equipment which equips by performing alignment of the above-mentioned circuit board and electronic parts, and junction. The pressurization press of the above-mentioned electronic parts is carried out at the above-mentioned circuit board, heating the above-mentioned anisotropy electric conduction film sheet. Correcting the curvature of the above-mentioned circuit board to coincidence, the above-mentioned anisotropy electric conduction film sheet which intervenes between the above-mentioned electronic parts and the above-mentioned circuit board is hardened, and the 10-13th ones possessing the equipment which joins the above-mentioned circuit board to the above-mentioned electronic parts of modes is provided with the mounting equipment of the electronic parts of a publication.

[0029] The equipment which will form the above-mentioned golden ball if this invention is caused like the 16th voice has the above-mentioned capillary tube from which a chamfer angle becomes 100 degrees or less while having the tip configuration which does not prepare a part even into the part which touches the above-mentioned golden ball, and it provides with the mounting equipment of the electronic parts of a publication the 10-15th ones by which a tip forms the profile conic above-mentioned golden bump in the above-mentioned electrode of the above-mentioned electronic parts of modes by this capillary tube.

[0030] The equipment which sticks on the circuit board or electronic parts the anisotropy conductive layer which blended the electric conduction particle with the insulating resin which blended the inorganic filler when this invention was caused like the 17th voice, The equipment which forms a ball at the tip of a metal wire by the electric spark like [the electrode of the above-mentioned electronic parts] wirebonding, and forms the bump who forms this in the above-mentioned electrode of the above-mentioned substrate by the capillary tube, and does not level it, With the equipment which carries out alignment of the above-mentioned electronic parts to the above-mentioned electrode of the above-mentioned circuit board, and carries them, and the tool heated by predetermined temperature Pressing the above-mentioned electronic parts with a pressure P1 to the above-mentioned circuit board as welding pressure, heating from the top face of the above-mentioned electronic parts, and correcting the curvature of the above-mentioned substrate The above-mentioned insulating resin which intervenes between the above-mentioned electronic parts and the

above-mentioned circuit board is hardened. Then, predetermined time of after, Dropping the above-mentioned welding pressure to the pressure P2 lower than the above-mentioned pressure P1, and easing the stress at the time of hardening of the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer The mounting equipment of the electronic parts characterized by having equipment which joins the above-mentioned circuit board to the above-mentioned electronic parts, and connects electrically the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board is offered.

[0031] if this invention is caused like the 18th voice, the above-mentioned pressure P1 will make the above-mentioned pressure P2 1/2 or less [of the above-mentioned pressure P1] more than 20gf(s) / bump -- the mounting equipment of the electronic parts of a publication is offered like the 17th voice.

[0032] If this invention is caused like the 19th voice, the 1-3rd ones which are characterized by the mean particle diameter of the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer being 3 micrometers or more of modes will be provided with the mounting approach of the electronic parts a publication.

[0033] the 1- which is two or more kinds of inorganic fillers with the mean particle diameter from which the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer differs if this invention is caused like the 20th voice -- either voice of 3 and 19 -- the mounting approach of the electronic parts a publication is offered like.

[0034] If this invention is caused like the 21st voice, the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer at least two kinds of inorganic fillers with the mean particle diameter from which plurality differs -- it is -- the above -- the mean particle diameter of one inorganic filler of two kinds of inorganic fillers, even if few the above -- the 1- from which the mean particle diameter of the inorganic filler of another side of two kinds of inorganic fillers differs more than twice even if few -- either voice of 3 and 19 -- the mounting approach of the electronic parts a publication is offered like.

[0035] If this invention is caused like the 22nd voice, the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer They are at least two kinds of inorganic fillers with the mean particle diameter from which plurality differs. Even if few, one inorganic filler of two kinds of inorganic fillers has the mean particle diameter exceeding 3 micrometers. the above -- the above -- the 1- in which the inorganic filler of another side of two kinds of inorganic fillers has the mean particle diameter of 3 micrometers or less even if few -- either voice of 3 and 19 -- the mounting approach of the electronic parts a publication is offered like.

[0036] If this invention is caused like the 23rd voice, the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer at least two kinds of inorganic fillers with the mean particle diameter from which plurality differs -- it is -- the above, when [of the mean particle diameter of two kinds of inorganic fillers] while is large and an inorganic filler consists of the same ingredient as the above-mentioned insulating resin even if few the 1- which does a stress relaxation operation so -- either voice of 3 and 19 -- the mounting approach of the electronic parts a publication is offered like.

[0037] If this invention is caused like the 24th voice, the above-mentioned inorganic filler blended with the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer They are at least two kinds of inorganic fillers with the mean particle diameter from which plurality differs. the above -- by being softer than the epoxy resin of the mean particle diameter of two kinds of inorganic fillers whose inorganic filler while is large and is the above-mentioned insulating resin, and compressing above-mentioned one inorganic filler, even if few the 1- which does a stress relaxation operation so -- either voice of 3 and 19 -- the mounting approach of the electronic parts a publication is offered like.

[0038] If this invention is caused like the 25th voice, the above-mentioned anisotropy conductive layer will provide with the mounting approach of the electronic parts a publication either mode of the 1-3rd, and 19-24 which the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate carried out as [be / than other parts / few above-mentioned amounts of inorganic fillers].

[0039] If this invention is caused like the 26th voice, the above-mentioned anisotropy conductive layer The 1st resin layer which was located in the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and blended the above-mentioned inorganic filler with the same insulating resin as the above-mentioned insulating resin, it has the 2nd resin layer which contacts the above-mentioned 1st resin layer, and consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 1st resin layer -- the mounting approach of the electronic parts a publication is offered

like the 25th voice.

[0040] If this invention is caused like the 27th voice, the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively will offer [having made it the above-mentioned anisotropy conductive layer have few above-mentioned amounts of inorganic fillers than other parts] the mounting approach of the electronic parts a publication like the 25th voice.

[0041] if this invention is caused like the 28th voice, the above-mentioned anisotropy conductive layer equips the opposite side with the 3rd resin layer which consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 1st resin layer further with the above-mentioned 2nd resin layer of the above-mentioned 1st resin layer, and the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer will contact the above-mentioned electronic parts and the above-mentioned substrate, respectively -- the mounting approach of the electronic parts a publication offers like the 26th voice.

[0042] if this invention is caused like the 29th voice, while the above-mentioned amount of inorganic fillers will make less than [20wt%] the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively, the above-mentioned amount of inorganic fillers of a part besides the above is more than 20wt% -- the mounting approach of the electronic parts a publication is offered like the 27th voice.

[0043] if this invention is caused like the 30th voice, while the above-mentioned amount of inorganic fillers will make each of the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer less than [20wt%], the above-mentioned amount of inorganic fillers of the above-mentioned 2nd resin layer is more than 20wt% -- the mounting approach of the electronic parts a publication is offered like the 28th voice.

[0044] If this invention is caused like the 31st voice, the above-mentioned anisotropy conductive layer will provide with the mounting approach of the electronic parts a publication either mode of the 1-3rd, and 19-24 made it whose above-mentioned amount of inorganic fillers decrease gradually or gradually toward other parts from the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate.

[0045] If this invention is caused like the 32nd voice, the above-mentioned anisotropy conductive layer will offer [having made it the above-mentioned amount of inorganic fillers decrease gradually or gradually toward other parts from the part which contacts, respectively in the above-mentioned electronic parts and the above-mentioned substrate] the mounting approach of the electronic parts a publication like the 31st voice.

[0046] If this invention is caused like the 33rd voice, while using the insulating resin which raises adhesion to the film material used for an electronic-parts front face, in the part in contact with the above-mentioned electronic parts, the mode of the 25th, 27, 29, or 31 that used the insulating resin which raises adhesion to the ingredient on the front face of a substrate will be provided with the mounting approach of the electronic parts a publication by the part in contact with the above-mentioned substrate.

[0047] If this invention is caused like the 34th voice, while using the insulating resin which raises adhesion to the film material used for an electronic-parts front face, in the above-mentioned resin layer in contact with the above-mentioned electronic parts, the mode of the 26th, 28, 30, or 32 that used the insulating resin which raises adhesion to the ingredient on the front face of a substrate will provide with the mounting approach of the electronic parts a publication by the above-mentioned resin layer in contact with the above-mentioned substrate.

[0048] If this invention is caused like the 35th voice, the above-mentioned anisotropy conductive layer will provide with the mounting approach of the electronic parts a publication either mode of the 1-3rd, and 19-24 with which it was made for the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate not to blend the above-mentioned inorganic filler.

[0049] If this invention is caused like the 36th voice, the above-mentioned anisotropy conductive layer The 1st resin layer which was located in the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and blended the above-mentioned inorganic filler with the same insulating resin as the above-mentioned insulating resin, it has the 2nd resin layer which consists of insulating resin which contacts the above-mentioned 1st resin layer, and does not blend the above-mentioned inorganic filler -- the mounting approach of the electronic parts a publication is offered like the 35th voice.

[0050] If this invention is caused like the 37th voice, the above-mentioned anisotropy conductive layer will offer [having made it the part which contacts, respectively not blend the above-mentioned inorganic filler with the above-mentioned electronic parts and the above-mentioned substrate] the mounting approach of the electronic parts a publication like the 35th voice.

[0051] if this invention is caused like the 38th voice, the above-mentioned anisotropy conductive layer is

further equipped with the 3rd resin layer which consists of insulating resin which does not blend the above-mentioned inorganic filler with the above-mentioned 2nd resin layer of the above-mentioned 1st resin layer in the opposite side, and the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer will contact the above-mentioned electronic parts and the above-mentioned substrate, respectively -- the mounting approach of the electronic parts a publication offers like the 36th voice.

[0052] if this invention is caused like the 39th voice, while making it the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively not blend the above-mentioned inorganic filler, the above-mentioned amount of inorganic fillers of a part besides the above is more than 20wt% -- the mounting approach of the electronic parts a publication is offered like the 37th voice.

[0053] if this invention is caused like the 40th voice, while making it each of the above-mentioned 1st resin layer and the above-mentioned 3rd resin layer not blend the above-mentioned inorganic filler, the above-mentioned amount of inorganic fillers of the above-mentioned 2nd resin layer is more than 20wt% -- the mounting approach of the electronic parts a publication is offered like the 38th voice.

[0054] If this invention is caused like the 41st voice, the above-mentioned anisotropy conductive layer The 4th resin layer which consists of insulating resin which was located in the part in contact with the above-mentioned electronic parts and the above-mentioned substrate, and blended the above-mentioned inorganic filler, Either mode equipped with the 5th resin layer which is located in the interstitial segment of the above-mentioned electronic parts and the above-mentioned substrate, and consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 4th resin layer of the 1-3rd, and 19-24 is provided with the mounting approach of the electronic parts a publication.

[0055] If this invention is caused like the 42nd voice, the above-mentioned anisotropy conductive layer The 4th resin layer which consists of insulating resin which was located in the part in contact with the above-mentioned electronic parts and the above-mentioned substrate, and blended the above-mentioned inorganic filler, Either mode equipped with the 5th resin layer which consists of insulating resin by which it is located in the interstitial segment of the above-mentioned electronic parts and the above-mentioned substrate, and the above-mentioned amount of inorganic fillers is not contained of the 1-3rd, and 19-24 is provided with the mounting approach of the electronic parts a publication.

[0056] If this invention is caused like the 43rd voice, the above-mentioned anisotropy conductive layer will provide with the mounting approach of the electronic parts a publication either mode of the 1-3rd, and 19-24 made it whose above-mentioned amount of inorganic fillers decrease gradually toward an interstitial segment with the above-mentioned electronic parts and the above-mentioned substrate from the part which contacts the above-mentioned electronic parts and the above-mentioned substrate, respectively.

[0057] if this invention is caused like the 44th voice -- the above-mentioned anisotropy conductive layer -- the near part of the above-mentioned electronic parts -- subsequently -- the near part of the above-mentioned substrate -- subsequently -- the order of the interstitial segment of the near part of the above-mentioned electronic parts, and the near part of the above-mentioned substrate -- the above-mentioned amount of inorganic fillers -- few -- having made -- either voice of the 1-3rd, and 19-24 -- the mounting approach of the electronic parts a publication is offered like.

[0058] the 43rd with which each amount of inorganic fillers of the near part of the above-mentioned electronic parts of the above-mentioned anisotropy conductive layer and the near part of the above-mentioned substrate was blended respectively corresponding to the coefficient of linear expansion of the part in contact with the above-mentioned anisotropy conductive layer of the coefficient of linear expansion of a part, and the above-mentioned substrate in contact with the above-mentioned anisotropy conductive layer of the above-mentioned electronic parts when this invention was caused like the 45th voice -- or the mounting approach of the electronic parts a publication is offered like 44 voice.

[0059] When this invention was caused like the 46th voice, where it made the anisotropy conductive layer which the bump formed in the electrode of electronic parts was blended in the inorganic filler at insulating resin, and was hardened in her intervene and the above-mentioned bump is crushed It was joined to the electrode of the circuit board and the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board are connected electrically. The above-mentioned anisotropy conductive layer The electronic-parts unit to which the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate is characterized by making it there be few above-mentioned amounts of inorganic fillers than other parts is offered.

[0060] When this invention was caused like the 47th voice, where it made the anisotropy conductive layer which the bump formed in the electrode of electronic parts was blended in the inorganic filler at insulating resin, and was hardened in her intervene and the above-mentioned bump is crushed It was joined to the

electrode of the circuit board and the above-mentioned electrode of the above-mentioned electronic parts and the above-mentioned electrode of the above-mentioned circuit board are connected electrically. The above-mentioned anisotropy conductive layer The 1st resin layer which was located in the part in contact with either the above-mentioned electronic parts or the above-mentioned substrate, and blended the above-mentioned inorganic filler with the same insulating resin as the above-mentioned insulating resin, The electronic-parts unit characterized by having the 2nd resin layer which contacts the above-mentioned 1st resin layer, and consists of insulating resin with few above-mentioned amounts of inorganic fillers than the above-mentioned 1st resin layer is offered.

[0061] If this invention is caused like the 48th voice, when impressing the above-mentioned supersonic wave and carrying out metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate, the mounting approach of electronic parts given in the 5th mode heated from both by the side of the above-mentioned electronic parts and the above-mentioned substrate is provided [while heating from the above-mentioned top-face side of the above-mentioned electronic parts, or], heating from the above-mentioned substrate side. if this invention is caused like the 49th voice -- the 1-9th and 19- either voice of 45 and 48 -- the electronic-parts unit by which the above-mentioned electronic parts were mounted in the above-mentioned substrate by the mounting approach of the electronic parts a publication like is offered.

[0062] If this invention is caused like the 50th voice, the above-mentioned bump will provide with the mounting approach of the electronic parts a publication either mode of the 1-9th, and 19-45 which is the bump who formed by plating or printing.

[0063] If this invention is caused like the 51st voice, the above-mentioned bump will provide with the electronic-parts unit of a publication the 46-49th ones which are the bump who formed by plating or printing of modes.

[0064] the 1-9th and 19- which blended the electric conduction particle which has a larger average diameter than the mean particle diameter of the above-mentioned inorganic filler with the solid insulating resin with which the above-mentioned anisotropy conductive layer blended the above-mentioned inorganic filler when this invention was caused like the 52nd voice -- either voice of 45 and 50 -- the mounting approach of the electronic parts a publication is offered like.

[0065] If this invention is caused like the 53rd voice, the above-mentioned anisotropy conductive layer will provide with the mounting equipment of the electronic parts of a publication the 10-18th ones by which the mean particle diameter of the above-mentioned inorganic filler blended the electric conduction particle which has a larger average diameter with the solid insulating resin which blended the above-mentioned inorganic filler of modes.

[0066] the 46- by which the mean particle diameter of the above-mentioned inorganic filler blended the electric conduction particle which has a larger average diameter with the solid insulating resin with which the above-mentioned anisotropy conductive layer blended the above-mentioned inorganic filler when this invention was caused like the 54th voice -- either voice of 49 and 51 -- the electronic-parts unit of a publication is offered like. If this invention is caused like the 55th voice, the equipment which impresses the above-mentioned supersonic wave and carries out the metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate is equipped with the heating component which heats from both by the side of the above-mentioned electronic parts and the above-mentioned substrate from an above-mentioned substrate side, and will provide [mode / which heated by above-mentioned heating component at time of the above-mentioned metal junction / 14th] the mounting equipment of the electronic parts of a publication from the above-mentioned top-face side of the above-mentioned electronic parts.

[0067]

[Embodiment of the Invention] Below, the gestalt of operation concerning this invention is explained at a detail based on a drawing.

[0068] (The 1st operation gestalt) It explains, referring to drawing 14 from drawing 1 (A), the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was hereafter mounted in the above-mentioned substrate by the mounting approach of the electronic parts concerning the 1st operation gestalt of this invention, the mounting approach of IC chip to the circuit board as an example of the equipment, its mounting equipment, and the above-mentioned mounting approach.

[0069] First, the IC chip mounting approach to the circuit board concerning the 1st operation gestalt of this invention is explained using drawing 1 (A) - drawing 4 (C), and drawing 6 (A) - (F).

[0070] In the IC chip 1 which is an example of the electronic parts of drawing 1 (A), a bump (projection

electrode) 3 is formed in aluminum pad electrode 2 of the IC chip 1 by actuation like drawing 3 (A) - drawing 3 (F) with wirebonding equipment. Namely, a ball 96 is formed in the lower limit of the wire 95 projected from the capillary tube 93 which is a holder in drawing 3 (A). Drop the capillary tube 93 which holds a wire 95 by drawing 3 (B), join a ball 96 to the electrode 2 of the IC chip 1, and the profile bump's 3 configuration is formed. A rise of a capillary tube 93 is started sending a wire 95 caudad by drawing 3 (C). The bump 3 as shows drawing 1 (B) and drawing 3 (F) is formed by forming and tearing off a bend 98 in a bump's 3 upper part, as a capillary tube 93 is moved to the loop formation 99 of a profile rectangle as shown in drawing 3 (D) and it is shown in drawing 3 (E). Or by clamping a wire 95 by the capillary tube 93 by drawing 3 (B), raising a capillary tube 93, and pulling up up A metal wire (gold streak) 95 (although there is a wire of the alloy which made tin, aluminum, copper, or these metals contain a trace element etc. as an example of a metal wire in addition, the following operation gestalten indicate as a golden wire (gold streak) as an example of representation.), for example, a golden wire It tears off and you may make it form the configuration of a bump 3 like drawing 3 (G). Thus, the condition of having formed the bump 3 is shown in each electrode 2 of the IC chip 1 at drawing 1 (B).

[0071] Subsequently, when equipping the circuit board 4 with the IC chip 1 with which the bump 3 was formed in each electrode 2, the anisotropy electric conduction film (ACF) sheet 10 is made to intervene as an example of an anisotropy conductive layer with this operation gestalt. This anisotropy electric conduction film sheet 10 contains inorganic filler 6f of an average diameter smaller than the average diameter of electric conduction particle 10a in the hard resin of insulating thermosetting which constitutes the anisotropy electric conduction film sheet 10. For example, as shown in drawing 36, when setting the average diameter of electric conduction particle 10a to 0.5 micrometers smaller than the average diameter of 1.0 micrometers of electric conduction particle 10a in the conventional ACF, the average diameter of an inorganic filler 6f particle is set to about 3-5 micrometers. As above-mentioned electric conduction particle 10a contained in the anisotropy electric conduction film sheet 10, what gold-plated at nickel powder is used. Thus, by constituting, the connection resistance between the electrode 5 by the side of a substrate and the bump 3 of IC tip side can be made to fall, and, in addition, it is suitable.

[0072] As above-mentioned electric conduction particle 10a, still more preferably By using the amount of electric conduction particle 10a as twice [more than] the anisotropy electric conduction film usually used widely using what carried out the coat to the outside of electric conduction particle body 10a-1 of the above-mentioned electric conduction particle 10a by insulating-layer 10a-2 Electric conduction particle 10a will be inserted into a bump 3 by a certain probability, and the resistance over the thermal shock by the swelling at the time of moisture absorption or the subsequent reflow can be improved.

[0073] Thus, if electric conduction particle 10a by which the insulating coat was carried out is put between the substrate electrodes 5 by the bump 3, very thin insulating coat partial 10a-2 of the outside of electric conduction particle 10a will be then shaved off, electric conduction particle body 10a-1 will be exposed, and it will demonstrate conductivity. Therefore, in the part which is not pinched by the electrode 5 with a bump 3, since insulating coat partial 10a-1 is not shaved off, conductivity is not demonstrated. Therefore, it will be said that it is hard to generate the short-circuit between an electrode 5 and an electrode 3 in the direction of a flat surface. Moreover, since electric conduction particles contact and between an electrode 3 and 5 may be made to short-circuit when it is made such, as described above, it is desirable [since it is usually difficult to put electric conduction particle 10a between an electrode 5 and a bump 3 since the area of the parietal region is small when a stud bump is used, it is required to put in many amounts of electric conduction particle 10a, but] to use the insulating electric conduction particle by which the insulating coat was carried out.

Moreover, also when the adhesives for anisotropy electric conduction film formation (or anisotropy electric conduction film sheet) expand to a Z direction (the thickness direction of an anisotropy electric conduction film sheet) by the swelling by temperature or humidity, a reflow property etc. becomes good, because electric conduction particle 10a expands more than it and can maintain connection. For this reason, it is desirable to use the plastics particle of a resilient Au-nickel coat etc. for electric conduction particle 10a.

[0074] Next, the anisotropy electric conduction film sheet 10 is stuck on a substrate 4 by the about two 5 - 10 kgf/cm pressure with the attachment tool 7 which has arranged the anisotropy electric conduction film sheet 10 with which it was cut into the bigger dimension a little than the magnitude of the IC chip 1, and inorganic filler 6f was blended on the electrode 5 of the circuit board 4 of drawing 1 (C) as shown in drawing 1 (D), for example, was heated by 80-120 degrees C. Then, the preparation process of a substrate 4 is completed by removing arranging [at the attachment tool side of the anisotropy electric conduction film sheet 10]-dismountable separator 10g. It is for preventing that the anisotropy electric conduction film sheet 10 containing the thermosetting resin of the solid-state which blended inorganic filler 6f with the tool 7, or a

semisolid sticks this separator 10g. As G part of drawing 1 (F) is expanded partially and shown in drawing 1 (G), here the anisotropy electric conduction film sheet 10 Spherical or the crushing silica of an average diameter smaller than the average diameter of electric conduction particle 10a, While what 6m of insulating resin was made to distribute inorganic system filler 6f, such as ceramics, such as an alumina, was mixed, carried out flattening of this with the doctor blade method etc., was made to evaporate a solvent component, and was solidified is desirable It is desirable to have the thermal resistance (for example, thermal resistance of extent which can bear 240 degrees C for 10 seconds) of extent which can bear the elevated temperature in the reflow process of a back process. Although the above-mentioned insulating resin can use what mixed insulating thermoplastics for for example, insulating thermosetting resin (for example, an epoxy resin, phenol resin, polyimide, etc.), insulating thermoplastics (for example, PONIFENIREN sulfide (PPS), a polycarbonate, modified polyphenylene oxide (PPO), etc.), or insulating thermosetting resin, it continues explanation as insulating thermosetting resin as an example of representation here. Generally the glass transition point of 6m of this thermosetting resin is about 120-200 degrees C. In addition, since the way of thermosetting resin functions dominantly in using what mixed thermoplastics for insulating thermosetting resin, while making it harden by suspending heating and making it cool naturally, after heating at first and making it once soften, when using only thermoplastics, it hardens by heating like thermosetting resin and a case.

[0075] Next, as shown in drawing 1 (E) and drawing 1 (F), it sets to the electronic-parts loading equipment 600 of drawing 20. Carrying out adsorption maintenance of the IC chip 1 with which the bump 3 was formed at the above-mentioned process from a tray 602 with the junction tool 8 by which the tip of the components attachment component 601 was heated Alignment of this IC chip 1 is carried out on the electrode 5 corresponding to the electrode 2 of the IC chip 1 of the substrate 4 which was prepared at the process before the above and laid on the stage 9, and the IC chip 1 is pressed to a substrate 4 through the anisotropy electric conduction film sheet 10. This alignment uses well-known location recognition actuation. For example, as shown in drawing 21 (C), the location recognition mark 605, lead, or land pattern formed in the substrate 4 is recognized with the camera 604 for substrate recognition of electronic-parts loading equipment 600. Based on the image 606 obtained with the camera 604 as shown in drawing 21 (D), XY coordinate location of the XY direction on the stage 9 of a substrate 4 which intersects perpendicularly, and the rotation location to the zero of XY coordinate are recognized, and the location of a substrate 4 is recognized on it. On the other hand, the mark 608 for location recognition or the circuit pattern of the IC chip 1 by which adsorption maintenance was carried out recognizes with the location recognition camera 603 for an IC chip to a junction tool 8, as shown in drawing 21 (A), the XY coordinate location of the above-mentioned XY direction of an IC chip 1 and the rotation location to the zero of a XY coordinate recognize based on the image 607 obtained with a camera 603 as shown in drawing 21 (B), and the location of an IC chip 1 recognizes on it. And the junction tool 8 or a stage 9 is moved based on the location recognition result of the above-mentioned substrate 4 and the IC chip 1, and after carrying out alignment so that it may be located on the electrode 5 of the substrate 4 with which the electrode 2 of the IC chip 1 corresponds, the IC chip 1 is pressed to a substrate 4 with the junction tool 8 by which heat was carried out [above-mentioned]. At this time, the bump 3 is pushed, while a bump's 3 head 3a deforms like drawing 4 (C) from drawing 4 (B) on the electrode 5 of a substrate 4. At this time, the sharp bump 3 who has entered into 6m of thermosetting resin at the time of junction initiation extrudes in a bump's 3 direction of an outside inorganic filler 6f in 6m of thermosetting resin also in this operation gestalt like drawing 2 (B) from drawing 2 (A) shown with the 1st operation gestalt. Moreover, like drawing 2 (C) shown with the 1st operation gestalt, when inorganic filler 6f does not enter between a bump 3 and the substrate electrode 5 according to the knockout operation to this direction of an outside in this operation gestalt, the effectiveness of reducing connection resistance is demonstrated. Though inorganic filler 6f enters somewhat between a bump 3 and the substrate electrode 5 at this time, there is no problem of a bump 3 and five substrate electrode by being directly in contact. Although the load impressed at this time changes with a bump's 3 outer diameters, it is made to surely deform the part which head 3a broke and lapped like drawing 4 (C). Moreover, as shown in drawing 6 (E), when metal plating is performed to electric conduction particle 10a in the anisotropy electric conduction film sheet 10 at the resin ball ball at this time, it is required for electric conduction particle 10a to deform. Moreover, it is required in the case of metal particles, such as nickel, for electric conduction particle 10a in the anisotropy electric conduction film sheet 10 to add a load which sinks into the electrode 5 by the side of a bump 3 or a substrate, as shown in drawing 6 (D). Also at the lowest, this load needs 20 (per gf / bump). That is, since it becomes large, resistance becomes large too much from resistance omega of 100mm /, and bump under by 20 (per gf / bump) and there is a problem practically from the graph of the

relation between the resistance in the case of a bump with an outer diameter of 80 micrometers, and a load, it is shown in drawing 17 that it is desirable that it is more than 20 (per gf / bump). Moreover, it is the graph which showed the reliable field to drawing 18 based on the relation between a with an outer diameter [each] (80 micrometers and 40 micrometers) bump and the minimum load. From this, by the bump with an outer diameter of 40 micrometers or more, as for the minimum load, it is desirable that it is more than 25 (per gf / bump), and it is presumed by the bump with an outer diameter of less than 40 micrometers that the minimum load is [more than 20 (per gf / bump)] reliable. In addition, when a bump outer diameter becomes [micrometers / less than 40] small with ** pitch-ization of a lead from now on, it is presumed that there is an inclination for a load to decrease in proportion to the square, according to a bump's projected area. Therefore, as for the minimum load impressed to a bump 3 side through the IC chip 1, it is desirable to need 20 (per gf / bump) at the lowest. Let the upper limit of the load impressed to a bump 3 side through the above-mentioned IC chip 1 be extent which the IC chip 1, a bump 3, the circuit board 4, etc. do not damage. By the case, the maximum load may exceed 100 (per gf / bump), or 150 (per gf / bump). If inorganic filler 6f of an average diameter smaller than the average diameter of an electric conduction particle is used at this time, while making the elastic modulus of 6m of thermosetting resin increase, the effectiveness of lowering a coefficient of thermal expansion can be demonstrated.

[0076] In addition, 10s of reference marks is resin with which heat curing of the 6m of the thermosetting resin under melting fused with the heat of the junction tool 8 among the anisotropy electric conduction film sheets 10 was carried out after melting among drawing.

[0077] With in addition, the junction tool 8 heated by built-in heater 8a, such as a ceramic heater or a pulse heater The alignment process which carries out alignment so that it may be located, as shown at drawing 1 R> 1 (E) on the electrode 5 of the substrate 4 with which the electrode 2 of the IC chip 1 corresponds to the substrate 4 with which the IC chip 1 formed on the electrode 2 was prepared for the bump 3 at the process before the above at the process before the above, One press [alignment-cum-] junction equipment, for example, the press [alignment-cum-] junction equipment of drawing 1 (E), may be made to perform the process which carries out press junction as shown in drawing 1 (F) after carrying out alignment. However, when producing continuously separate equipment, for example, many substrates, in order to raise productivity by doing an alignment activity and a press junction activity instantaneous, the alignment equipment of drawing 5 (B) performs the above-mentioned alignment process, and the junction equipment of drawing 5 R> 5 (C) may be made to perform the above-mentioned press junction process. In addition, since productivity is raised, two junction equipments 8 are shown and it can be made to carry out in drawing 5 R> 5 (C) at coincidence press junction of the two places of the circuit board 4 of one sheet.

[0078] In the above and each following operation gestalt, a multilayered ceramic substrate, a glass fabric laminating epoxy group plate (GARAEPO substrate), an aramid nonwoven fabric substrate, a glass fabric laminating polyimide resin substrate, FPC (flexible printed circuit), or an aramid nonwoven fabric epoxy group plate (for example, resin multilayer substrate currently sold as trademark ARIBU "ALIVH" by Matsushita Electric Industrial Co., Ltd.) is used as the circuit board 4.

[0079] These substrates 4 have produced curvature and a wave by the heat history, and decision and processing, and are not necessarily perfect flat surfaces. Then, as shown in drawing 5 (A) and drawing 5 (B), the curvature of the circuit board 4 of the impressed part is corrected by the junction tool 8 and stage 9 where parallelism was managed, respectively so that it might be adjusted to about 10 micrometers or less by impressing heat and a load to the circuit board 4 locally through the IC chip 1 towards a stage 9 side from the junction tool 8 side.

[0080] Moreover, although the IC chip 1 has curved considering the core of an active side as concave, both the curvatures and waves of a substrate 4 and the IC chip 1 are reformable by pressurizing this by the strong load of 20 or more gves per one bump at the time of junction. The curvature of this IC chip 1 is generated with the internal stress produced in case a thin film is formed in Si, when forming the IC chip 1. A bump's deformation is about 10-25 micrometers, and it can approve now because each bump 3 adapts herself to the effect of a wave which appears in a front face from the inner layer copper foil which the substrate of this level has from the beginning by deformation of a bump 3.

[0081] In this way, it is in the condition that the curvature of the circuit board 4 was corrected, for example, 140-230-degree C heat is impressed to the anisotropy electric conduction film sheet 10 between the IC chip 1 and the circuit board 4 several seconds to about 20 seconds, for example, and this anisotropy electric conduction film sheet 10 is hardened. At this time, 6m of thermosetting resin which constitutes the anisotropy electric conduction film sheet 10 at first flows, and it closes to the edge of the IC chip 1. Moreover, since it softens automatically at the beginning when it is heated, since it is resin, a fluidity which

flows to an edge in this way arises. By making the volume of 6m of thermosetting resin larger than the volume of the space between the IC chip 1 and the circuit board 4, it can flow out so that this space may be overflowed, and the closure effectiveness can be done so. Then, it is fixed on the circuit board 4 by 10s of resin which the IC chip 1 constituted the anisotropy electric conduction film sheet 10, and was hardened as the temperature of the IC chip 1 and the anisotropy electric conduction film sheet 10 falls rapidly since the source of heating is lost when the heated junction tool 8 goes up, the anisotropy electric conduction film sheet 10 lost a fluidity and it was shown in drawing 1 (F) and drawing 4 (C). Moreover, if the circuit board 4 side is heated by heater 9a of a stage 9 etc., temperature of the junction tool 8 can be made lower.

[0082] If it does in this way, by being able to use the thermosetting resin which blended the inorganic filler of mean particle diameter smaller than the average diameter of electric conduction particle 10a with the anisotropy electric conduction film sheet 10, and using what gold-plated further at nickel powder as electric conduction particle 10a contained in the anisotropy electric conduction film sheet 10, connection resistance can be made to fall and, in addition, it is suitable.

[0083] According to the above-mentioned 1st operation gestalt, dependability can be improved more by blending inorganic filler 6f with the mean particle diameter smaller than the average diameter of electric conduction particle 10a as inorganic filler 6f blended with 6m of thermosetting resin, without checking work of electric conduction particle 10a. That is, electric conduction particle 10a is inserted between a bump 3 and the electrode 5 of a substrate 4. At this time, even if inorganic filler 6f is inserted into coincidence, since that mean particle diameter is smaller than the average diameter of electric conduction particle 10a, conductivity is not checked, moreover, the modulus of elasticity which is 6m of thermosetting resin is increased, a coefficient of thermal expansion is fallen, and the junction dependability of the IC chip 1 and a substrate 4 is improved.

[0084] (The 2nd operation gestalt) Next, it explains, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 2nd operation gestalt of this invention, for example, IC chip.

[0085] Let the inorganic filler 6f mixed rate blended with the anisotropy electric conduction film sheet 10 containing thermosetting resin be what of the 6m of the above-mentioned insulating thermosetting resin, for example, an insulating thermosetting epoxy resin, is much more suitable as 5 - 90wt% in the 1st operation gestalt in this 2nd operation gestalt. While there is no semantics which mixes inorganic filler 6f and adhesive strength will fall to the degree of pole if 90wt% is exceeded, since sheet-izing becomes difficult, it is not desirable less than [5wt%]. 20 - 40wt%, while 40 - 70wt% is desirable, about 20wt% can reduce the coefficient of linear expansion of sheet encapsulant considerably, and it is [about] effective [in a resin substrate, / with a GARAEPOL substrate,] from a viewpoint which maintains high dependability as an example, in a resin substrate with a ceramic substrate. in addition -- volume % -- wt% -- about -- one half -- comparatively -- or an epoxy resin -- 1 -- receiving -- silica about 2 specific gravity -- comparatively -- carrying out . In usual, a this inorganic filler 6f mixed rate is determined as the conditions on the manufacture at the time of sheet-izing of 6m of thermosetting resin, the elastic modulus of a substrate 4, and the last target by the dependability test result.

[0086] By blending with the anisotropy electric conduction film sheet 10 containing thermosetting resin inorganic filler 6f of a mixed rate which was described above, the modulus of elasticity of 6m of thermosetting resin of the anisotropy electric conduction film sheet 10 can be made to be able to increase, a coefficient of thermal expansion can be reduced, and the junction dependability of the IC chip 1 and a substrate 4 can be raised. Moreover, according to the ingredient of a substrate 4, an inorganic filler 6f mixed rate can be determined so that the ingredient constant of 6m of thermosetting resin, i.e., an elastic modulus, and coefficient of linear expansion may be made the optimal. In addition, although an elastic modulus becomes large as an inorganic filler 6f mixed rate carries out flower arrangement, coefficient of linear expansion tends to become small.

[0087] In the 1st operation gestalt and the 2nd operation gestalt, while being easy to deal with it in order to use the anisotropy electric conduction film sheet 10 of the solid-state instead of a liquid, since there is no liquid component, it can form with a macromolecule, and there is an advantage of being easy to form the high thing of a glass transition point.

[0088] In addition, it sets from drawing 1 (A) to drawing 1 (G) and drawing 2 (A) - drawing 2 (C), drawing 6 mentioned later, and drawing 7 . Although it explained forming the anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b for anisotropy electric conduction film formation containing the

thermosetting resin as an example of an anisotropy conductive layer in a circuit board 4 side As shown in not the thing limited to this but drawing 14 (A), or drawing 14 (B), after forming in the IC chip 1 side, you may make it join to a substrate 4. In this case, in the case of the anisotropy electric conduction film sheet 10 which contains thermosetting resin especially, the IC chip 1 held by the attachment components 200, such as an adsorption nozzle, at the elastic bodies 117, such as rubber on a stage 201, with separator 6a arranged dismountable at the circuit board side of the anisotropy electric conduction film sheet 10 is pushed, and the anisotropy electric conduction film sheet 10 may be made to be stuck on the IC chip 1 in accordance with a bump's 3 configuration.

[0089] (The 3rd operation gestalt) Next, it explains using drawing 6 (A) - drawing 6 (C) and drawing 7 (A) - drawing 7 (F), the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 3rd operation gestalt of this invention, for example, IC chip.

[0090] Instead of sticking the anisotropy electric conduction film sheet 10 containing thermosetting resin on a substrate 4 in the 1st operation gestalt with this 3rd operation gestalt, as shown in drawing 6 (A) and drawing 7 (A), and (D) the semisolid condition spreading according thermosetting adhesive 6b for anisotropy electric conduction film formation of the shape of a liquid as an example of an anisotropy conductive layer to dispensing 502 etc. to a circuit board 4 top, or after printing or making it imprint, the so-called B stage condition, and until solidification -- carrying out -- ** Then, the above-mentioned IC chip 1 is carried in the above-mentioned substrate 4 like the above-mentioned 1st or 2nd operation gestalt.

[0091] spreading by the dispensing 502 movable to the 2-way which discharge quantity is controlled by pneumatic pressure as shows liquid-like thermosetting adhesive 6b for anisotropy electric conduction film formation on the circuit board 4 at drawing 7 (A), and intersects perpendicularly on a substrate flat surface in detail as shown in drawing 6 (A) etc. -- or it prints or imprints. subsequently -- while impressing heat and a pressure and equalizing with the tool 78 which contained heater 78a like drawing 6 (B) -- drawing 6 (C) -- like -- a semisolid condition and the so-called B stage condition -- until solidification is carried out.

[0092] Or after applying thermosetting adhesive 6b of a liquid to the predetermined location on a substrate 4 by the dispenser 502 as shown in drawing 7 (A) when the viscosity of liquid-like thermosetting adhesive 6b for anisotropy electric conduction film formation is low, since the viscosity of thermosetting adhesive 6b is low, it will be in the condition that it is automatically shown in breadth and drawing 7 (B) on a substrate. Then, as shown in drawing 7 (C), it solidifies to semisolid-izing, i.e., the so-called B stage condition, by putting in the above-mentioned substrate 4 in a furnace 503 by transport device 505 like a conveyor, and stiffening liquid thermosetting adhesive 6b of the insulating resin by which spreading was carried out [above-mentioned] at the heater 504 of a furnace 503.

[0093] On the other hand, since it does not spread on a substrate automatically [since the viscosity of thermosetting adhesive 6b is high] after applying thermosetting adhesive 6b of a liquid to the predetermined location on a substrate 4 by the dispenser 502 as shown in drawing 7 (D) when the viscosity of liquid-like thermosetting adhesive 6b for anisotropy electric conduction film formation is high, as shown in drawing 7 (E) and (F), it extends to Taira and others by the squeegee 506. then, the thing for which the above-mentioned substrate 4 is put in in a furnace 503 by transport device 505 like a conveyor, and liquid thermosetting adhesive 6b of the insulating resin by which spreading was carried out [above-mentioned] at the heater 504 of a furnace 503 is stiffened as shown in drawing 7 (C) -- semisolid-izing, i.e., the so-called B stage condition, -- until solidification is carried out.

[0094] Thus, when semisolid-izing thermosetting adhesive 6b for anisotropy electric conduction film formation, a difference is pressed with the property of the thermosetting resin in thermosetting adhesive 6b at 80-130 degrees C which is 30 - 80% of temperature of the glass transition point of this thermosetting resin of a certain thing. Usually, it carries out at about 30% of temperature of the glass transition point of thermosetting resin. Thus, from the graph of whenever [stoving temperature / of the anisotropy electric conduction film sheet of drawing 1919], and conversion, if the reason made into 30 - 80% of the glass transition point of thermosetting resin is within the limits of 80-130 degrees C, it can still leave the range which reacts further at a back process fully. If in other words it is the temperature within the limits of 80-130 degrees C, it will be based also on time amount, but since the conversion of insulating resin, for example, an epoxy resin, can control to about 10 - 50%, a problem does not arise in the junction at the time of IC chip sticking by pressure of a back process. That is, when pressing at the time of IC chip sticking by pressure, the predetermined amount of press can be secured and it is hard to produce the problem of it becoming impossible to force one's way. In addition, it may semisolid-ize by suppressing a reaction and

making only a part for a solvent evaporate.

[0095] In equipping a substrate 4 with two or more IC chips 1 after making it semisolid-ize as the above-mentioned thermosetting adhesive 6b was described above In two or more parts equipped with two or more IC chips 1 of a substrate 4, make a semisolid chemically-modified [of the above-mentioned thermosetting adhesive 6b / above-mentioned] degree into a preceding paragraph picking process, and it is performed beforehand. Thus, productivity becomes high more by joining two or more IC chips 1 to the substrate 4 supplied by supplying the substrate 4 which picked the preceding paragraph in two or more above-mentioned parts. At a next process, even when using thermosetting adhesive 6b, the same process as the process using the anisotropy electric conduction film sheet 10 of the 1st or 2nd operation gestalt fundamentally described above is performed. By adding a semipermanent chemically-modified [above-mentioned] degree, thermosetting adhesive 6b for anisotropy electric conduction film formation of a liquid can be used like the anisotropy electric conduction film sheet 10, and a solid-state, therefore since there is no liquid component while being easy to deal with it, it can form with a macromolecule, and there is an advantage of being easy to form the high thing of a glass transition point. Thus, in using thermosetting adhesive 6b for anisotropy electric conduction film formation with a fluidity, it compares with the case where the solid anisotropy electric conduction film sheet 10 is used, and also doubles and has the advantage which can be applied, printed or imprinted in the magnitude of arbitration in the location of the arbitration of a substrate 4.

[0096] (The 4th operation gestalt) Next, it explains using drawing 22, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 4th operation gestalt of this invention, for example, IC chip. When the point that the 4th operation gestalt differs from the 1st operation gestalt joins the IC chip 1 to a substrate 4, In addition to a load, also impress a supersonic wave, and it presses by the load of 20 or less gves if needed, without leveling a bump 3. After preparing a bump tip so that short-circuit with the contiguity bump or electrode of the neck (mustache) part at the above-mentioned bump's 3 tip which was lengthened at the time of bump formation and produced by julienning twisted for falling may be prevented, It is carrying out alignment to the IC chip 1, carrying the IC chip 1 in a substrate 4, and carrying out ultrasonic concomitant use thermocompression bonding of the metal bump 3 to the metal of the electrode surface by the side of a substrate. The condition of joining the IC chip 1 to a substrate 4 is the same as that of drawing 2 in a previous operation gestalt, drawing 6, etc. You may make [while heating from the above-mentioned top-face side of the above-mentioned IC chip 1, or] it heat from both by the side of the above-mentioned IC chip 1 and the above-mentioned substrate, when impressing the above-mentioned supersonic wave and carrying out metal junction of the above-mentioned golden bump 3 and the above-mentioned electrode of the above-mentioned substrate 4, heating from the above-mentioned substrate side.

[0097] The thing made to semisolid-ize as thermosetting adhesive 6b for anisotropy electric conduction film formation of the anisotropy electric conduction film sheet 10 of the solid-state which blended inorganic filler 6f with 6m of insulating thermosetting resin, or a liquid was described above with this 4th operation gestalt is stuck on a substrate 4. Or after making a substrate 4 apply and semisolid-ize thermosetting adhesive 6b for anisotropy electric conduction film formation containing thermosetting resin, A ball 96 is formed at the tip of a gold streak 95 by the electric spark by actuation like drawing 3 (A) - drawing 3 (F) like [the electrode 5 of the circuit board 4, and the electrode 2 of electronic parts 1] wirebonding. Without leveling the bump 3 formed by carrying out ultrasonic thermocompression bonding of this ball 96 to the substrate electrode 5 by the capillary tube 93, alignment is carried out to the IC chip 1, and the IC chip 1 is carried in a substrate 4. Here, the one half solid state of the thermosetting adhesive 6b for anisotropy electric conduction film formation of a liquid which was explained with the 3rd operation gestalt is carried out, and the above "the thing made to semisolid-ize as thermosetting adhesive 6b for anisotropy electric conduction film formation of a liquid was described above" is almost the same as what was formed into B stage. At this time, in the ultrasonic impression equipment 620 shown in drawing 22 with the junction tool 628 beforehand heated at the built-in heater 622 The load by the air cylinder 625 from the top face of the IC chip 1 by which this junction tool 628 was adsorbed, Metal junction of the gold plate by the side of the golden bump 3 and a substrate is carried out preparing a tip so that the supersonic wave which is generated by ultrasonic generating component 623 like a piezo-electric element, and is impressed through the ultrasonic horn 624 may be made to act and **** of the golden bump's 3 neck part may be prevented. next, the top face of the IC chip 1 -- or -- and the above-mentioned IC chip 1 being pressed with the welding pressure of 20 or more gves per one bump to the above-mentioned circuit board 4, heating from a substrate side, and,

crushing correction and the bump 3 of the curvature of the above-mentioned substrate 4. The above-mentioned IC chip 1, the above-mentioned anisotropy electric conduction film sheet 10 which intervenes between the above-mentioned circuit boards 4, or thermosetting adhesive 6b is hardened with the above-mentioned heat, the above-mentioned circuit board 4 is joined to the above-mentioned IC chip 1, and two electrodes 2 and 5 are connected electrically. In addition, you may make it heat [side / above-mentioned / substrate / both / by the side of the above-mentioned IC chip 1 and the above-mentioned substrate] from the above-mentioned top-face side of the above-mentioned IC chip 1 at the time of the above-mentioned metal junction by ultrasonic impression equipment 620. That is, specifically it may heat at the built-in heater 622 from the above-mentioned top-face side of the above-mentioned IC chip 1, a circuit board 4 side may be heated by heater 9a of a stage 9 from the above-mentioned substrate side, or you may make it heat by the built-in heater 622 and heater 9a of a stage 9 from both by the side of the above-mentioned IC chip 1 and the above-mentioned substrate.

[0098] In addition, since it is hard coming to generate frictional heat also in the junction which used the supersonic wave in this way, the reason which needs the welding pressure of 20 or more gves per one bump is because it becomes impossible to join. When joining gold and gold, a bump is pushed by a certain fixed load, by impressing a supersonic wave there, frictional heat arises and metals are joined. Therefore, it is needed, the fixed load of extent, i.e., the welding pressure of 20 or more gves per one bump, which presses a bump also in this case. As an example of welding pressure, they may be 50 or more gves per one bump.

[0099] According to the above-mentioned 4th operation gestalt, since metal diffusion junction of the metal plating of a substrate 4 is carried out with the metal bump 3, it is suitable when it seems that he wants to make connection resistance still lower, a case so that he may want to give the reinforcement in a bump part more, and.

[0100] (The 5th operation gestalt) Next, it explains using drawing 8 (A) - drawing 8 (C) and drawing 9 (A) - drawing 9 (C), the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 5th operation gestalt of this invention, for example, IC chip. It differs in that the 5th operation gestalt can abbreviate a closure process to the 1st operation gestalt.

[0101] As described above, the projection electrode (bump) 3 is formed in the electrode 2 on the IC chip 1. To the circuit board 4 As shown in drawing 8 (B), drawing 8 (C), drawing 9 (A), and drawing 23 The anisotropy electric conduction film sheet 10 of the shape of a sheet of the rectangle of a geometry smaller than the dimension OL of the profile rectangle which connected the toe edge of two or more electrodes 2 of the IC chip 1, or thermosetting adhesive 6b is stuck or applied to a part for the core which tied the electrode 5 of the circuit board 4. It is made for that volume to become larger than the clearance between the IC chip 1 and a substrate 4 at this time as for the thickness of the sheet-like anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b. Moreover, the up-and-down cutter 641 cuts to a geometry smaller than the dimension OL of the profile rectangle which connected the toe edge of two or more electrodes 2 of the IC chip 1 in the part in which the anisotropy electric conduction film sheet 656 of the shape of a sheet of the rectangle which is rewound from the rewinding roll 644 by the attachment equipment 640 of drawing 23, twists, and is rolled round by the roll 643 was beforehand put into the end eye 657. The anisotropy electric conduction film sheet 10 of the shape of a sheet of the cut rectangle is stuck on a part for the core which was beforehand heated at the built-in heater 646 and which stuck, and adsorption maintenance was carried out with the head 642, and tied the electrode 5 of the above-mentioned circuit board 4. Next, the IC chip 1, the anisotropy electric conduction film sheet 10 which intervenes between the circuit boards 4, or thermosetting adhesive 6b is hardened, carrying out the pressurization press of the IC chip 1 with the junction tool 8 heated by heater 8a at the circuit board 4, and correcting the curvature of a substrate 4 to coincidence, as alignment of the electrode 5 of the circuit board 4 is carried out to a bump 3 and it is shown in drawing 8 (A) and drawing 9 (B). At this time, it softens, as described above with the heat applied through the IC chip 1 from the junction tool 8, and the anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b is pressurized from the location stuck or applied like drawing 9 (C), and flows out toward an outside. This anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b that flowed out becomes a closure ingredient (under-filling), and improves remarkably the dependability of junction to a bump 3 and an electrode 5. Moreover, when a certain fixed time amount is formed, in the above-mentioned anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b, hardening will advance gradually and the circuit board 4 will be joined to the IC chip 1 by 6s of resin finally hardened. By going up, junction of the IC chip 1 and the electrode 5 of the circuit board 4 completes the junction tool 8 which is pressing the IC chip

1. In the case of heat curing, if it says strictly, the reaction of thermosetting resin progresses, while heating, and most fluidities will be lost while the junction tool 8 goes up. Since the anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b has not covered the electrode 5 before junction according to the approach which was described above, in case it joins, a bump 3 contacts an electrode 5 directly, the anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b does not enter the bottom of an electrode 5, but the connection resistance between a bump 3 and an electrode 5 can be made low. Moreover, if the circuit board side is heated, temperature of the junction head 8 can be made lower. If this approach is applied to the above-mentioned 3rd operation gestalt, junction to a golden bump and the golden electrode (they are nickel and the gold-plated thing to copper or a tungsten) of the circuit board can carry out more easily.

[0102] (The 6th operation gestalt) Next, it explains using drawing 10 - drawing 11, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 6th operation gestalt, for example, IC chip. In the 6th operation gestalt, a different point from the 1st operation gestalt is a point that reliable junction can also be attained, when a bump 103 is shifted and mounted in the electrode 5 of the circuit board 4.

[0103] In the 6th operation gestalt, as shown in drawing 10 (A), in case a bump 3 is formed on the IC chip 1, the golden ball 96 is formed for a gold streak 95 by the electric spark like wirebonding. Next, adjusting the magnitude of a ball by the time amount when carrying out an electric spark The time amount for generating an electric spark for ball 96a of diameter phid-Bump which formed ball 96a of diameter phid-Bump shown by 95a, and was formed in this way, or the parameter of an electrical potential difference is controlled. Ball 96a is fabricated so that chamfer diameter phiD which chamfer angle thetaC shows by 93a of the capillary tube 193 100 degrees or less may be set to 1/2 to 3/4 of golden ball diameter d-Bump. The bump 3 as prepares even part 93b in the part which touches the golden ball of a capillary tube 93 as shown in drawing 10 (C) and shows drawing 10 (D) is not formed. By the capillary tube 193 which made at least the point which does not establish an even part in the part which touches golden ball 96a of a capillary tube 193 as shown in drawing 10 (A) the tip configuration which has 193a The bump 103 as shows at drawing 10 (B) is formed in the electrode 2 of the IC chip 1 by ultrasonic thermocompression bonding. By using the capillary tube 193 of the above-mentioned tip configuration, a tip like b of drawing 10 (B) can form the profile conic bump 103 in the electrode 2 of the IC chip 1. Since a bump 103 is a profile cone form when the tip formed by the above-mentioned approach is shifted and mounted in the electrode 5 of the circuit board 4 like drawing 11 (C) in the profile conic bump 103, when the tip is gap to the one half of a bump's 103 outer diameter, some bumps 103 can surely contact the electrode 5 of a substrate 4.

[0104] On the other hand, although 3g of a part of so-called plinths of the width method d contacts an electrode 5 by the bump 3 as shows drawing 11 (D) as a bump 3 is shown in drawing 11 (E), when only a dimension Z is shifted and mounted in the electrode 5 of the circuit board 4 like drawing 11 (C), it does not contact partially and a contact condition serves as unstable junction. the case where such a substrate 4 is covered over a cold energy impact test or a reflow with such an unstable junction condition -- the above -- junction of an unstable junction condition may have become opening (i.e., poor junction). On the other hand, since a bump 103 is a cone form when the profile conic bump 103 shifts [a tip] to the electrode 5 of the circuit board 4 and only a dimension Z is mounted with the above-mentioned 6th operation gestalt, as shown in drawing 1111 (C), When it is gap to the one half of a bump's 103 outer diameter, some bumps 103 can surely contact the electrode 5 of a substrate 4, and even when it applies to a cold energy impact test or a reflow, it can prevent that joining becomes poor.

[0105] (The 7th operation gestalt) Next, it explains using drawing 12 - drawing 13, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 7th operation gestalt, for example, IC chip. It enables it to ease the stress of the IC chip 1 and the circuit board 4 in the 1st operation gestalt with this 7th operation gestalt at the time of hardening of thermosetting resin after the IC chip 1 to the circuit board 4 joins.

[0106] In the 7th operation gestalt, alignment is carried out to the electrode 5 of the circuit board 4, without leveling the bump 3 formed in the electrode 2 of the IC chip 1 of the above-mentioned wirebonding, making the anisotropy electric conduction film sheet 10 of the solid-state which blended inorganic filler 6f with 6m of insulating thermosetting resin, or a semisolid, or thermosetting adhesive 6b intervene. For example, in the

case of a ceramic substrate, the above-mentioned IC chip 1 is pressed with the welding pressure beyond pressure P1=80gf per one bump at the above-mentioned circuit board 4, heating the IC chip 1 from the rear face with the tool 8 heated by the constant temperature of about 230 degrees C, and the above-mentioned IC chip 1, the above-mentioned anisotropy electric conduction film sheet 10 which intervenes between the above-mentioned circuit boards 4, or thermosetting adhesive 6b is hardened with the above-mentioned heat, correcting the curvature of the above-mentioned substrate 4. Next, after fixed time amount t1, although it changes with the conversion of 20 seconds, then an ingredient, whole time amount After 5 seconds of the 1/4 or 1/2 - 10 seconds, in other words, before the conversion of an ingredient reaches to 90%, it lowers to the pressure P2 lower than the above-mentioned pressure P1, the stress at the time of hardening of thermosetting adhesive 6b is eased, the above-mentioned circuit board 4 is joined to the above-mentioned IC chip 1, and two electrodes 2 and 5 are connected electrically. While obtaining a pressure required [in order for the bump to deform] for deformation and adaptation of a bump since 20gf extent is indispensable suitably In order to extrude excessive resin from between the IC chip 1 and substrates 4, while the above-mentioned pressures P1 are more than 20gf(s) / bump, in order [which was unevenly distributed inside resin before deformation of a bump etc.] to carry out hardening distortion removal, dependability's improve more by making a pressure P2 into under 20gf(s) / bump. The reason is as [detailed] follows. That is, as shown in drawing 12 (C), the stress distribution of the thermosetting resin in the anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b is large by the IC chip 1 and substrate 4 side at the time of sticking by pressure. By as [this], when fatigue is repeatedly given by the reliability trial or the usual long-term use, the thermosetting resin in the anisotropy electric conduction film sheet 10 or thermosetting adhesive 6b may exfoliate in an IC chip 1 or substrate 4 side, without the ability finishing bearing stress. When it will be in such a condition, the adhesive strength of the IC chip 1 and the circuit board 4 becomes less enough, and a joint will open. Like drawing 13 then, by using two steps of pressure profiles of the higher pressure P1 and the lower pressure P2 It can lower to the pressure P2 lower than the above-mentioned pressure P1 at the time of hardening of thermosetting adhesive 6b. Like drawing 12 (D), it was unevenly distributed inside resin at the time of a pressure P2, and hardening distortion removal is carried out and the stress of the IC chip 1 and the circuit board 4 is eased (in other words). While obtaining a pressure required for deformation and adaptation of a bump by being able to reduce the concentration degree of stress and raising to the above-mentioned pressure P1 after that, excessive resin can be extruded from between the IC chip 1 and substrates 4, and dependability improves.

[0107] in addition, the above "adhesive strength of the IC chip 1 and the circuit board 4" should adhere the IC chip 1 and a substrate 4 -- the thing of **** is meant. IC1 and the substrate 4 are joined by these [of the adhesive strength according / this / to adhesives, the hardening shrinkage force when hardening adhesives, and the shrinkage force (for example, shrinkage force when contracting, when the adhesives heated by 180 degrees C return to ordinary temperature) of a Z direction] three force.

[0108] (The 8th opération gestalt) Next, it explains using drawing 12 - drawing 13 , the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 8th operation gestalt, for example, IC chip. It is made for the above-mentioned inorganic filler 6f mean particle diameter blended with the 6m of the above-mentioned insulating resin to be 3 micrometers or more in each above-mentioned operation gestalt with this 8th operation gestalt. However, the above-mentioned inorganic filler 6f maximum mean diameter is taken as the magnitude which does not exceed the clearance dimension after junction to the IC chip 1 and a substrate 4.

[0109] If mean particle diameter uses a less than 3-micrometer fine particle as inorganic filler 6f when blending inorganic filler 6f with 6m of insulating resin, the surface area of those particles itself may become large as a whole, and it may absorb moisture to the surroundings which are inorganic filler 6f whose mean particle diameter is a less than 3-micrometer fine particle, and is not desirable in junction to the IC chip 1 and a substrate 4.

[0110] Therefore, in blending inorganic filler 6f of the same weight, mean particle diameter can make the surrounding amount of moisture absorption of inorganic filler 6f become less by using 3 micrometers or more big inorganic filler 6f, and it becomes possible to raise moisture resistance of it. Moreover, generally, since the inorganic filler with big mean particle diameter (if it puts in another way average grain size) is cheaper, it is desirable also in cost.

[0111] In addition, by the method of construction which uses conventional ACF (Anisotropic Conductive Film: anisotropy electric conduction film)598 in junction to the IC chip 1 and a substrate 4, as shown in

drawing 24 (A), while surely inserting the electric conduction particle 599 in ACF598 between a bump 3 and the substrate electrode 5, an electric conduction particle with a diameter of 3-5 micrometers is crushed to the diameter of 1-3 micrometers, and it is necessary to demonstrate conductivity. however, with each above-mentioned operation gestalt of this invention Since it is stuck by pressure, crushing a bump 3 with the substrate electrode 5 as there is no need of not necessarily inserting between a bump 3 and the substrate electrode 5 and it is shown in drawing 24 (B) even if there is electric conduction particle 10a It will escape from and come out from a bump 3, the substrate electrode 4, and between also inorganic filler 6f with the anisotropy conductive layer 10 between a bump 3 and the substrate electrode 4 at the time of this sticking by pressure. When unnecessary inorganic filler 6f is caught between the substrate electrode 4 and a bump 3, based on the description of hardly checking conductivity, inorganic filler 6f with a big mean particle diameter of 3 micrometers or more can be used. Namely, even if electric conduction particle 10a should not be inserted between a bump 3 and the substrate electrode 5, but with a diameter of 3-5 micrometers electric conduction particle 10a should be crushed to the diameter of 1-3 micrometers with this operation gestalt and it does not demonstrate conductivity It is stuck by pressure, crushing a bump 3 with the substrate electrode 5, and since the bump 3 contacted the substrate electrode 5 directly electrically and has acquired electric conductivity, in any way, it is satisfactory and dependability can be improved, without being influenced by the inorganic filler. That is, in the direct junction to a bump 3 and the substrate electrode 5, the above-mentioned electric conduction particle 10a does so a contingent effect [say / that the connection resistance between the electrode 5 by the side of a substrate and the bump 3 of IC tip side can be made to fall], when electric conduction particle 10a is inserted between a bump 3 and the substrate electrode 5.

[0112] (The 9th operation gestalt) Next, it explains using drawing 25 and 26, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 9th operation gestalt of this invention, for example, IC chip. Drawing 25 and 26 are the partial expansion type section Figs. of the anisotropy electric conduction film sheet 10 used the type section Fig. of the junction condition manufactured by the mounting approach of the electronic parts to the circuit board concerning the above-mentioned 9th operation gestalt, for example, IC chip, and equipment, respectively, and then. With this 9th operation gestalt, inorganic filler 6f-1 with the mean particle diameter from which plurality differs, and 6f-2 cost the above-mentioned inorganic filler 6f blended with the 6m of the above-mentioned insulating resin of the above-mentioned anisotropy conductive layer 10 in each above-mentioned operation gestalt. As an example, it considers as an inorganic filler with the mean particle diameter of 0.5 micrometers, and an inorganic filler with the mean particle diameter of 2-4 micrometers.

[0113] By mixing inorganic filler 6f-1 with the mean particle diameter from which plurality differs, and 6f-2 to 6m of insulating resin according to the above-mentioned 9th operation gestalt The inorganic filler 6f amount mixed to 6m of insulating resin can be made to be able to increase, the surrounding amount of moisture absorption of an inorganic filler can be made to become less, and while becoming possible to raise moisture resistance, film-izing (solid state) becomes easy. That is, when it thinks by weight %, the direction into which it was intermingled and the inorganic filler from which particle size differs was put rather than one kind of inorganic filler is able to increase the amount of the inorganic filler per unit volume. By this, the anisotropy electric conduction film sheet 10 as a closure sheet or inorganic filler 6f [to adhesives 6b for anisotropy electric conduction film formation] loadings can be increased, the coefficient of linear expansion of the anisotropy electric conduction film sheet 10 or adhesives 6b for anisotropy electric conduction film formation can be reduced, reinforcement can be carried out more, and dependability can be raised.

[0114] Next, it sets, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 10th operation gestalt of this invention, for example, IC chip. (The 10th operation gestalt) In order to make effectiveness in the above-mentioned 9th operation gestalt into a more positive thing, further One mean particle diameter of inorganic filler 6f-1 of inorganic filler 6f-1 with the above-mentioned mean particle diameter from which plurality differs, and 6f-2 differs in the mean particle diameter of inorganic filler 6f-2 of another side more than twice. As an example, it considers as an inorganic filler with the mean particle diameter of 0.5 micrometers, and an inorganic filler with the mean particle diameter of 2-4 micrometers.

[0115] By doing in this way, the effectiveness in the above-mentioned 9th operation gestalt can be heightened further. Namely, one mean particle diameter of inorganic filler 6f-1 By mixing inorganic filler

6f-1 with the mean particle diameter from which the plurality from which the mean particle diameter of inorganic filler 6f-2 of another side differs more than twice differs, and 6f-2 to 6m of insulating resin The inorganic filler 6f amount mixed to 6m of insulating resin can be made to increase more certainly. Filmizing (solid state) becomes easier and the anisotropy electric conduction film sheet 10 or inorganic filler 6f [to adhesives 6b for anisotropy electric conduction film formation] loadings is increased. The coefficient of linear expansion of the anisotropy electric conduction film sheet 10 or adhesives 6b for anisotropy electric conduction film formation can be reduced more, and can carry out reinforcement more, and dependability can be raised more.

[0116] Next, it sets, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 11th operation gestalt of this invention, for example, IC chip. (The 11th operation gestalt) In order to make effectiveness in the above-mentioned 9th operation gestalt into a more positive thing, further the above-mentioned inorganic filler 6f blended with the 6m of the above-mentioned insulating resin It is at least two kinds of inorganic filler 6f-1 with the mean particle diameter from which plurality differs, and 6f-2. the above -- the mean particle diameter to which one inorganic filler 6f-1 of two kinds of inorganic fillers exceeds 3 micrometers even if few -- having -- the above -- even if few, as for inorganic filler 6f-2 of another side of two kinds of inorganic fillers, it is desirable to have the mean particle diameter of 3 micrometers or less. As an example, it considers as an inorganic filler with the mean particle diameter of 0.5 micrometers, and an inorganic filler with the mean particle diameter of 2-4 micrometers.

[0117] Next, it sets, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 12th operation gestalt of this invention, for example, IC chip. (The 12th operation gestalt) In each above-mentioned operation gestalt, further the above-mentioned inorganic filler 6f blended with the 6m of the above-mentioned insulating resin It is at least two kinds of inorganic filler 6f-1 with the mean particle diameter from which plurality differs, and 6f-2. the above -- even if few, when [of the mean particle diameter of two kinds of inorganic fillers] while is large and inorganic filler 6f-1 consists of the same ingredient as the 6m of the above-mentioned insulating resin, a stress relaxation operation can be done so. As an example, it considers as an inorganic filler with the mean particle diameter of 0.5 micrometers, and an inorganic filler with the mean particle diameter of 2-4 micrometers.

[0118] According to this 12th operation gestalt, when in addition to the operation effectiveness in the 9th operation gestalt while is large as for mean particle diameter, inorganic filler 6f-1 consists of the same ingredient as the 6m of the above-mentioned insulating resin and stress acts on the 6m of the above-mentioned insulating resin, as for mean particle diameter, while is large, and when inorganic filler 6f-1 unites with the 6m of the above-mentioned insulating resin, a stress relaxation operation can be done so.

[0119] Next, it sets, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the 13th operation gestalt of this invention, for example, IC chip. (The 13th operation gestalt) In each above-mentioned operation gestalt, further the above-mentioned inorganic filler 6f blended with the 6m of the above-mentioned insulating resin It is at least two kinds of inorganic filler 6f-1 with the mean particle diameter from which plurality differs, and 6f-2. the above -- even if few, it is softer than the epoxy resin of the mean particle diameter of two kinds of inorganic fillers whose inorganic filler 6f-1 while is large and is the 6m of the above-mentioned insulating resin, and a stress relaxation operation can be done so by compressing above-mentioned one inorganic filler 6f-1.

[0120] According to this 13th operation gestalt, in the operation effectiveness in the 9th operation gestalt in addition, when [of mean particle diameter] while is large and inorganic filler 6f-1 consists of the same ingredient as the 6m of the above-mentioned insulating resin Since it is large and softer than the epoxy resin whose inorganic filler 6f-1 is the 6m of the above-mentioned insulating resin when stress acts on the 6m of the above-mentioned insulating resin, A stress relaxation operation can be done so by being compressed by the above-mentioned stress so that above-mentioned one inorganic filler 6f-1 shows drawing 27, and distributing the tensile force which is the reaction force over compression in the perimeter.

[0121] Next, it sets, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board

concerning the 14th operation gestalt of this invention, for example, IC chip. (The 14th operation gestalt) As shown in drawing 28 (A), (B), drawing 29 (A), (B), drawing 30, and drawing 31, in each above-mentioned operation gestalt, further the above-mentioned anisotropy conductive layer 10 The part 700 in contact with the above-mentioned IC chip 1 or the above-mentioned substrate 4 or layer 6x have few above-mentioned amounts of inorganic fillers than other parts 701 or layer 6y, or can be prevented from blending the above-mentioned inorganic filler 6f. In this case, without distinguishing clearly the part 700 in contact with the above-mentioned IC chip 1 or the above-mentioned substrate 4, and other parts 701, as shown in drawing 28 (A) and (B), you may make it the amount of inorganic fillers change gradually, and may make it distinguish clearly, as shown in drawing 29 (A), (B) and drawing 30, and drawing 31. In drawing 29 R>9 (A), (B) and drawing 30, and drawing 31 namely, the above-mentioned anisotropy conductive layer 10 the 1st which was located in the part in contact with the above-mentioned IC chip 1 or the above-mentioned substrate 4, and blended the above-mentioned inorganic filler 6f with the same insulating resin as the 6m of the above-mentioned insulating resin -- with resin layer 6x the above 1st -- resin layer 6x -- contacting -- and the above 1st -- rather than resin layer 6x, it is few, or the above-mentioned amount of inorganic fillers can be equipped with 2nd resin layer 6y constituted by the above-mentioned insulating resin which does not blend the above-mentioned inorganic filler 6f, and can also make it multilayer structure.

[0122] The following effectiveness can be done so if it does in this way. That is, if the above-mentioned inorganic filler 6f is put in by the same percent by weight (wt%) as the whole anisotropy conductive layer, inorganic filler 6f may increase IC tip side side, a substrate side, or near the opposed face of the both, and it will decrease conversely in the interstitial segment of the IC chip 1 and a substrate 4. Consequently, IC tip side side, a substrate side, or near the opposed face of those both, since there is much inorganic filler 6f, the adhesive strength between the anisotropy conductive layer 10, the IC chip 1, a substrate 4, or its both may decline. According to the above-mentioned 14th operation gestalt, when the part 700 in contact with either the above-mentioned IC chip 1 or the above-mentioned substrate 4 or layer 6x have few above-mentioned amounts of inorganic fillers than other parts 701 or layer 6y or it is made not to blend the above-mentioned inorganic filler 6f, since there are many amounts of inorganic fillers, it can prevent that adhesive strength declines.

[0123] Below, the various modifications of this 14th operation gestalt are explained.

[0124] First, as for the above-mentioned anisotropy conductive layer 10, the part 700 which contacts both the above-mentioned IC chip 1 and the above-mentioned substrate 4, respectively has few above-mentioned amounts of inorganic fillers than other parts 701, or it can avoid blending the above-mentioned inorganic filler 6f as the 1st modification, as shown in drawing 28 (C), drawing 29 (C), and drawing 32 (A). Without distinguishing clearly the part 700 in contact with both the above-mentioned IC chip 1 and the above-mentioned substrate 4, and other parts 701, as shown in drawing 28 (C) also in this case, you may make it the amount of inorganic fillers change gradually, and may make it distinguish clearly, as shown in drawing 29 (C) and drawing 32 (A). In drawing 29 (C) and drawing 32 (A) namely, the above-mentioned anisotropy conductive layer 10 the above 1st -- the above-mentioned 2nd resin layer 6y of resin layer 6x -- the opposite side -- the above 1st -- whether there are few above-mentioned amounts of inorganic fillers than resin layer 6x or 3rd resin layer 6z which consists of above-mentioned insulating resin which does not blend the above-mentioned inorganic filler 6f -- further -- having -- multilayer structure -- carrying out -- the above 1st -- resin layer 6x and the above-mentioned 3rd resin layer 6z can contact the above-mentioned IC chip 1 and the above-mentioned substrate 4, respectively.

[0125] furthermore, the part 700 which contacts the above-mentioned IC chip 1, the above-mentioned substrate 4, or its both as another modification, respectively -- the above-mentioned amount of inorganic fillers -- less than [20wt%] -- or while making it not blend the above-mentioned inorganic filler 6f, the above-mentioned amount of inorganic fillers of the part 701 besides the above can be more than 20wt%. In this case, without distinguishing clearly the part 700 in contact with the above-mentioned IC chip 1, the above-mentioned substrate 4, or both, and other parts 701, as shown in drawing 28 (A), (B), and (C), you may make it the amount of inorganic fillers change gradually, and may make it distinguish clearly, as shown in drawing 29 (A), (B), drawing 29 (C), drawing 30, drawing 31, and drawing 32 (A). namely, the above 1st -- resin layer 6x or the 1st -- resin layer 6x and the above-mentioned 3rd resin layer 6z -- the above-mentioned amount of inorganic fillers -- less than [20wt%] -- or while making it not blend the above-mentioned inorganic filler 6f, the above-mentioned amount of inorganic fillers of the above-mentioned 2nd resin layer 6y can be more than 20wt%.

[0126] As an example, when the above-mentioned 2nd resin layer 6y considers as a thermosetting epoxy resin as 6m of insulating resin, in the case of a ceramic substrate, it is 50wt(s)% and, in the case of a

GARAEPO substrate, is made into 20wt(s)%. moreover -- as an example -- the 1st -- the thickness of resin layer 6x or 3rd resin layer 6z or its both sets thickness of 15 micrometers and 2nd resin layer 6y to 40-60 micrometers. Moreover, as the thickness of the above-mentioned anisotropy conductive layer 10 is completely filled between the IC chip 1 and a substrate 4 at the time of junction to the IC chip 1 and a substrate 4 as a bigger dimension than the clearance dimension after junction to the IC chip 1 and a substrate 4, it makes junction a more positive thing.

[0127] Moreover, it may be made to make reverse the loadings of the modification shown in drawing 28 (C), drawing 29 (C), and drawing 32 (A), and an inorganic filler as another modification. That is, the above-mentioned anisotropy conductive layer 10 has few above-mentioned amounts of inorganic fillers than the part 703 to which the interstitial segment 702 of a part 703 which contacts both the above-mentioned IC chip 1 and the above-mentioned substrate 4, respectively contacts both the above-mentioned IC chip 1 and the above-mentioned substrate 4, respectively, or can be prevented from blending the above-mentioned inorganic filler 6f, as shown in drawing 28 (D). Without distinguishing clearly the part 703 which contacts the above-mentioned IC chip 1, the above-mentioned substrate 4, or both also in this case, and an interstitial segment 702, you may make it the amount of inorganic fillers change gradually, and may make it distinguish clearly, as shown in drawing 29 (D) and drawing 32 (B). As shown in drawing 29 (D) and drawing 32 (B), namely, the above-mentioned anisotropy conductive layer 10 4th resin layer 6v which consists of 6m of insulating resin which was located in the part in contact with the above-mentioned IC chip 1 and the above-mentioned substrate 4, and blended the above-mentioned inorganic filler 6f, or [that it is located in the interstitial segment of the above-mentioned IC chip 1 and the above-mentioned substrate 4, and there are few above-mentioned amounts of inorganic fillers than the above-mentioned 4th resin layer 6v] -- or it can have 5th resin layer 6w which consists of 6m of insulating resin which is not contained.

[0128] or [thus, / that there are few above-mentioned amounts of inorganic fillers at the above-mentioned interstitial segment 702 of the above-mentioned IC chip 1 and the above-mentioned substrate 4, or above-mentioned 5th resin layer 6w than the part 703 or the above-mentioned 4th resin layer 6v which contacts the above-mentioned IC chip 1 and the above-mentioned substrate 4, respectively if it carries out] -- or since it is not contained, an elastic modulus becomes low and can do the stress relaxation effectiveness so.

Moreover, if it is used as insulating resin of the part 703 or the above-mentioned 4th resin layer 6v which contacts, respectively, choosing the high thing of the adhesion force to the IC chip 1 and a substrate 4 as the above-mentioned IC chip 1 and the above-mentioned substrate 4 In above-mentioned 4th resin layer 6v of the part 703 in contact with the above-mentioned IC chip 1, or the near part of the IC chip 1 While choosing inorganic filler 6f loadings or an ingredient so that it may become as close to the coefficient of linear expansion of the IC chip 1 as possible In above-mentioned 4th resin layer 6v of the part 703 in contact with the above-mentioned substrate 4, or the near part of a substrate 4, inorganic filler 6f loadings or an ingredient can be chosen so that it may become as close to the coefficient of linear expansion of a substrate 4 as possible. Consequently, in order that the coefficient of linear expansion of the above-mentioned 4th resin layer 6v of the part 703 in contact with the above-mentioned IC chip 1 or the near part of the IC chip 1 and the IC chip 1 may approach, while being hard coming to generate exfoliation between both, in order that the coefficient of linear expansion of the above-mentioned 4th resin layer 6v of the part 703 in contact with the above-mentioned substrate 4 or the near part of a substrate 4 and a substrate 4 may approach, it is hard coming to generate exfoliation between both.

[0129] Furthermore, as a continuous line shows to drawing 33 (A) and (B), the above-mentioned amount of inorganic fillers of the above-mentioned anisotropy conductive layer 10 can decrease gradually or gradually toward other parts P2 from the part P1 in contact with either the above-mentioned IC chip 1 or the above-mentioned substrate 4.

[0130] Moreover, as a continuous line shows to drawing 33 (C) and (D), the above-mentioned amount of inorganic fillers of the above-mentioned anisotropy conductive layer 10 can increase gradually or gradually toward other parts P5, i.e., the interstitial segment of the IC chip 1 and the above-mentioned substrate 4, from the parts P3 and P4 which contact, respectively in the above-mentioned IC chip 1 and the above-mentioned substrate 4.

[0131] Moreover, as a continuous line shows to drawing 33 (E), the above-mentioned amount of inorganic fillers of the above-mentioned anisotropy conductive layer 10 can decrease gradually toward an interstitial segment (part equivalent to the interstitial segment 702 in the modification of drawing 28 (D)) with the above-mentioned IC chip 1 and the above-mentioned substrate 4 from the part (part equivalent to the contact part 703 in the modification of drawing 28 (D)) which contacts, respectively in the above-mentioned IC chip 1 and the above-mentioned substrate 4.

[0132] moreover, a continuous line shows to drawing 33 (F) -- as -- the above-mentioned anisotropy conductive layer 10 -- the near part of the above-mentioned IC chip 1 -- subsequently -- the near part of the above-mentioned substrate 4 -- subsequently -- the order of the interstitial segment of the near part of the above-mentioned IC chip 1, and the near part of the above-mentioned substrate 4 -- the above-mentioned amount of inorganic fillers -- few -- making . In addition, although it has illustrated that the above-mentioned amount of inorganic fillers changes gradually in order of the above in drawing 33 (F), it is not restricted to this and you may make it change gradually.

[0133] or [that there are few above-mentioned amounts of inorganic fillers at the interstitial segment of the above-mentioned IC chip 1 and the above-mentioned substrate 4 than the part which contacts the above-mentioned IC chip 1 and the above-mentioned substrate 4, respectively if it carries out like the modification of above-mentioned drawing 33 (E) and (F)] -- or since it is not contained, an elastic modulus becomes low and can do the stress relaxation effectiveness so. Moreover, if it is used as insulating resin of the part which contacts, respectively, choosing the high thing of the adhesion force to the IC chip 1 and a substrate 4 as the above-mentioned IC chip 1 and the above-mentioned substrate 4 While choosing inorganic filler 6f loadings or an ingredient so that it may become as close to the coefficient of linear expansion of the IC chip 1 as possible in the part in contact with the IC chip 1, in the part in contact with a substrate 4 Inorganic filler 6f loadings or an ingredient can be chosen so that it may become as close to the coefficient of linear expansion of a substrate 4 as possible. when inorganic filler 6f loadings are determined in this viewpoint, a continuous line usually shows to drawing 33 (F) -- as -- the near part of the above-mentioned IC chip 1 -- subsequently -- the near part of the above-mentioned substrate 4 -- subsequently to the order of the interstitial segment of the near part of the above-mentioned IC chip 1, and the near part of the above-mentioned substrate 4, the above-mentioned amount of inorganic fillers becomes as [be / few]. In order that the coefficient of linear expansion of the part and the IC chip 1 which contact the IC chip 1 by considering as such a configuration may approach, while being hard coming to generate exfoliation between both, in order that the coefficient of linear expansion of the part and substrate 4 in contact with a substrate 4 may approach, it is hard coming to generate exfoliation between both.

[0134] Drawing 33 (A) It is desirable to make the above-mentioned amount of inorganic fillers into 5 - 90wt% of within the limits practically in any [of - (F)] case. In less than [5wt%], while there is no semantics which mixes inorganic filler 6f and adhesive strength will fall to the degree of pole if 90wt% is exceeded, since sheet-sizing becomes difficult, it is because it is not desirable.

[0135] in addition, since 6m of insulating resin become soft and fuse with the heat at the time of junction and the above-mentioned resin layer be mix when thermocompression bonding of the IC chip 1 be carry out to a substrate 4, use the film of the multilayer structure which consist of two or more resin layers 6x and 6y, or above 6x, 6y and 6z as an anisotropy conductive layer, finally, the boundary where each resin layer be clear be lose, and it become the inorganic filler distribution which inclined like drawing 33 .

[0136] Furthermore, in the above-mentioned 14th operation gestalt or each modification, it is also possible to use different insulating resin according to the above-mentioned part or a resin layer in the anisotropy conductive layer which has inorganic filler 6f the part or layer which entered, or the anisotropy conductive layer toward which inorganic filler distribution inclined. For example, in the part or resin layer in contact with the IC chip 1, while using the insulating resin which raises adhesion to the film material used for IC chip front face, in the part or resin layer in contact with a substrate 4, it also becomes possible to use the insulating resin which raises adhesion to the ingredient on the front face of a substrate.

[0137] According to the above-mentioned 14th operation gestalt and those various above-mentioned modifications, inorganic filler 6f does not exist in the junction interface of the IC chip 1 or the above-mentioned substrate 4, and the anisotropy conductive layer 10, or there are few the amounts. The adhesive property of insulating resin original can be demonstrated, adhesive high insulating resin can increase in number in the above-mentioned junction interface, the IC chip 1 or the above-mentioned substrate 4, and 6m [of insulating resin] adhesion reinforcement can be raised, and an adhesive property with the IC chip 1 or the above-mentioned substrate 4 improves. Thereby, while the life in various reliability trials improves, the peel strength to bending improves.

[0138] Although it does not contribute to the adhesion itself, if inorganic filler 6f with the effectiveness of lowering coefficient of linear expansion is distributed by homogeneity in 6m of insulating resin, inorganic filler 6f will contact a substrate 4 or IC chip front face, the amount of the adhesives contributed to adhesion will decrease, and an adhesive fall is caused. Consequently, if exfoliation arises between the IC chip 1 or a substrate 4, and adhesives, moisture invades from there and it becomes causes, such as corrosion of the electrode of the IC chip 1. Moreover, if peeling advances from an exfoliation part, the junction of the IC

chip 1 and a substrate 4 itself will become poor, and it will serve as a faulty connection electrically. [0139] On the other hand, according to the above-mentioned 14th operation gestalt and those various above-mentioned modifications, adhesive strength can be raised, giving the effectiveness of lowering the coefficient of linear expansion by inorganic filler 6f, as described above. By this, adhesion reinforcement with the IC chip 1 and a substrate 4 improves, and dependability improves.

[0140] Furthermore, when few inorganic filler 6f parts 700 or resin layer 6x have been arranged to IC tip side, or when inorganic filler distribution is made small in IC tip side, it becomes possible to raise the adhesion force of the part 700 or resin layer 6x concerned to the passivation film which consists of the silicon nitride and oxidization silicon of IC chip front face. Moreover, it also becomes possible to choose suitably the insulating resin which raises adhesion to the film material used for these IC chip front face, and to use it. Moreover, the stress concentration in the inside of the closure sheet material which is an example of an anisotropy conductive layer is eased by lowering the elastic modulus near the IC chip. If the ingredient used for a substrate 4 takes such structure like a ceramic in being hard (an elastic modulus is high), an elastic modulus with the closure sheet material near the substrate and coefficient of linear expansion match, and, in addition, it is suitable.

[0141] On the other hand, when few inorganic filler 6f parts 700 or resin layer 6x have been arranged to the substrate side or when inorganic filler distribution is made small at a substrate side [when bending joins a substrate 4 like a resin substrate or a flexible substrate (FPC)] In case a substrate 4 is built into the case of electronic equipment, when bending stress is added, the adhesion reinforcement of a substrate 4 and the closure sheet which is an example of an anisotropy conductive layer can be used in order to improve. When the surface layer of IC tip side consists of a protective coat formed by the polyimide film, generally adhesion of insulating resin is good, and by applying to a substrate 4 and changing from the IC chip 1 continuously [a modulus of elasticity and coefficient of linear expansion] or gradually, when not becoming a problem, a closure sheet is hard at IC tip side, and it can consider as a soft ingredient by the substrate side. Thereby, since stress generating inside a closure sheet becomes small, dependability improves.

[0142] Furthermore, when inorganic filler 6f few parts 700 or the resin layers 6x and 6z have been arranged on IC tip side and both sides by the side of a substrate, or when inorganic filler distribution is made small in IC tip side and the both sides by the side of a substrate While being able to reconcile two cases the above-mentioned IC tip side and by the side of a substrate and being able to raise the adhesion in both by the side of IC tip side and a substrate, coefficient of linear expansion can be lowered and both of a substrate 4 can be connected to the IC chip 1 with high dependability. Moreover, according to the quality of the material and the substrate quality of the material of IC tip side front face, insulating resin with more good adhesion and resin ***** can be chosen and used. Moreover, since little thing inclination with many these inorganic filler 6f amounts is freely changeable, it is making very thin few inorganic filler 6f parts or layers, and matching with a substrate ingredient is possible for it.

[0143] (The 15th operation gestalt) Next, in the 15th operation gestalt of this invention, the production process of the anisotropy conductive layer used, the electronic-parts unit or module, for example, the semiconductor device, with which the above-mentioned IC chip was mounted in the above-mentioned substrate by the mounting approach, the equipment, and the above-mentioned mounting approach of the electronic parts to the circuit board concerning the above-mentioned 8-14th operation gestalten and those modifications, for example, IC chip, is explained based on drawing 34 and drawing 35.

[0144] First, in forming an anisotropy conductive layer on the circuit board 4 directly, the 1st resin sheet is stuck on the circuit board 4, and it sticks the 2nd resin sheet on it. At this time, when there is much inorganic filler 6f, it becomes like drawing 28 (A) or drawing 30 at the 1st resin sheet, and in being reverse, it becomes like drawing 28 (B) or drawing 31. namely, the part 700 with little [are a resin sheet corresponding to the part 701 with much above-mentioned inorganic filler 6f on the 1st resin sheet, or 2nd resin layer 6y in the case of the former, and / in the case of the latter] above-mentioned inorganic filler 6f or the 1st -- it becomes a resin sheet corresponding to resin layer 6x.

[0145] moreover, the part 700 with few [form the 3rd resin sheet further on the 2nd resin sheet, and / inorganic filler 6f] the 1st resin sheets and the 3rd resin sheets or the 1st -- in corresponding to resin layer 6x, it becomes like drawing 28 (C) or drawing 32 (A).

[0146] moreover, the 1st resin sheet 673 and the 2nd resin sheet 674 are shown in this order only in this case at (drawing 34 and drawing 35 on the base film 672 beforehand called a separator in these as shown in drawing 34 and drawing 35 .) -- or this may also stick and form the 3rd resin sheet conversely or further. In this case, it sticks like drawing 34 R>4 and drawing 35 , heating two or more resin sheets 673,674 if needed with the roller 670,270 which can heat a vertical pair. Then, if the formed resin sheet object 671 is cut for

every predetermined dimension, it will become the above-mentioned anisotropy electric conduction film sheet 10 as shown in drawing 28 (A) - (C) and drawing 29 (A) - (C) or drawings 30 -32.

[0147] Moreover, in case the anisotropy electric conduction film sheet object with which the anisotropy electric conduction film sheet 10 continued is produced as another modification, the epoxy which was able to be melted to the solvent, and an inorganic filler are applied on the base film called a separator by a doctor blade method etc. This solvent is dried and an anisotropy electric conduction film sheet object is manufactured.

[0148] At this time, inorganic filler 6f concentration is low, or it applies on a base film, using as the 1st layer the insulating liquid-like resin in which inorganic filler 6f is not contained, and that 1st-layer applied desiccation is once performed depending on the case. In not drying, a little, inorganic filler of 2nd layer 6f mixes in the 1st layer, and inorganic filler 6f becomes the structure toward which inorganic filler distribution inclined as shown in drawing 33 .

[0149] On the 1st layer by which spreading formation was carried out [above-mentioned], the insulating resin of the shape of a liquid which mixed more inorganic filler 6f than the 1st layer is applied, and it may be the 2nd layer. By drying the 2nd layer, the two-layer fabric anisotropy electric conduction film sheet object with which the 1st layer and the 2nd layer were formed on the base film can be formed. If an anisotropy electric conduction film sheet object is cut for every predetermined dimension, it will become the above-mentioned anisotropy electric conduction film sheet 10 as shown in drawing 28 (A), drawing 29 (A), and drawing 30 .

[0150] In addition, when inorganic filler 6f arranges few layers to a substrate side, after forming the 2nd layer on a process contrary to the above, i.e., a base film, the 1st layer is formed on the 2nd layer and a two-layer fabric anisotropy electric conduction film sheet object can be formed. If an anisotropy electric conduction film sheet object is cut for every predetermined dimension, it will become the above-mentioned anisotropy electric conduction film sheet 10 as shown in drawing 28 (B), drawing 29 (B), and drawing 31 .

[0151] moreover, with inorganic filler 6f low concentration once Or it is spreading desiccation (it may be omitted), using as the 1st layer 6m of insulating resin in which inorganic filler 6f is not contained. It carries out, the insulating resin which mixed many inorganic filler 3f rather than the 1st layer on the 1st layer is applied, and it is spreading desiccation (it may be omitted) as the 2nd layer. It carries out, and on this, or there are few amounts of an inorganic filler than the 2nd layer, the 3rd layer which is not is applied. By drying this, the anisotropy electric conduction film sheet object of a three-tiered structure with which the 1st layer, the 2nd layer, and the 3rd layer were formed on the base film can be formed. If an anisotropy electric conduction film sheet object is cut for every predetermined dimension, it will become the above-mentioned anisotropy electric conduction film sheet 10 as shown in drawing 28 (C), drawing 29 (C), and drawing 32 (A).

[0152] While choosing the resin of the optimal ingredient for electronic parts and arranging to an electronic-parts side in the above-mentioned anisotropy conductive layer directly [above-mentioned] by the side which manufactures the above-mentioned electronic-parts unit according to the approach of forming an anisotropy conductive layer on the circuit board 4, the resin of the optimal ingredient for a substrate can be chosen, it can arrange to a substrate side, and the degree of freedom of selection of resin can be raised.

[0153] On the other hand, by the approach of manufacturing an anisotropy electric conduction film sheet object, there is no degree of freedom of selection so that it described above, but it can do [manufacturing many above-mentioned anisotropy electric conduction film sheets 10 collectively or], and while manufacture effectiveness is good and becoming cheap, attachment equipment becomes enough [one set].

[0154] As described above, according to each above-mentioned operation gestalt of this invention, many of processes conventionally taken to join the circuit board to electronic parts, for example, IC chip, can be abolished, and productivity can be raised very much. That is, a sealing agent is poured in, and after carrying out flip chip junction, for example, it is necessary to put into a batch type furnace and to harden in junction by the stud bump bonding and the solder bump who indicated as a conventional example. Hardening of several minutes and a sealing agent takes 2 to 5 hours per piece at impregnation of this sealing agent. In stud bump bonding mounting, after supposing further that it is the previous line, imprinting Ag paste by the bump and carrying this in a substrate, the process of hardening Ag paste is needed. This process takes 2 hours. On the other hand, by the approach of the above-mentioned operation gestalt, the above-mentioned closure process can be abolished and productivity can be raised very much. Furthermore, with the above-mentioned operation gestalt, by using the closure sheet of the insulating resin of a solid-state or a semisolid etc., an epoxy resin with big molecular weight can be used, it can become joinable in a short time for about 10 - 20 seconds, compaction of a jointing time can also be aimed at, and productivity can be raised further.

Furthermore, the following effectiveness can also be done so.

[0155] (1) It is necessary to perform the bump formation process of dedication by chip makers, and a bump's formation can be performed only by the limited manufacturer by the approach (conventional example 3) of forming a bump formation bump by plating. However, according to the above-mentioned operation gestalt of this invention, with wirebonding equipment, general-purpose IC chip for wirebonding can be used, and acquisition of IC chip becomes easy. That is, the reason for the ability to use general-purpose IC chip for wirebonding is that wirebonding equipment and bump bonding equipment can be used and a bump can form on the usual IC pad with which aluminum pad was formed if it is wirebonding. On the other hand, on aluminum pad, in order to form a plating bump by the approach (conventional example 3) of forming a bump by plating, after forming barrier metals, such as Ti, Cu, and Cr, a resist is applied and exposed on a spin coat and only the bump formation section makes a hole. It forms by energizing the electrical and electric equipment to this, and performing plating which becomes a part for the hole from Au etc. Therefore, since a large-scale gilding machine and the plant for waste disposal of the dangerous substance, such as cyanides, are needed in order to form a plating bump, at the works which perform the usual assembly process, it cannot carry out actually.

[0156] Moreover, compared with the approach of the conventional example 1, bump leveling for stabilizing the amount of imprints of the adhesives in the unstable imprint process of the imprint of electroconductive glue becomes unnecessary, and becomes unnecessary [such leveling equipment for leveling processes]. In order to crush the reason on the electrode of a substrate, pressing a bump, it is because it is not necessary to level only a bump beforehand.

[0157] Moreover, if it is made to be the following in the above-mentioned operation gestalt, reliable junction can also be attained when a bump 103 is shifted and mounted in the electrode 5 of the circuit board 4. That is, in case a bump 3 is formed on the IC chip 1, golden ball 96a is formed for a gold streak by the electric spark like wirebonding. Next, form ball 96a of diameter phid-Bump shown by 95a, and chamfer diameter phiD which shows this by 93a of the capillary tube 193 from which chamfer angle thetac becomes 100 degrees or less is set to 1/2 to 3/4 of diameter d-Bump of golden ball 96a. A bump 103 is formed in the electrode 2 of the IC chip 1 by the supersonic wave and thermocompression bonding by the capillary tube 193 made into the tip configuration which does not establish an even part in the part which touches golden ball 96a of a capillary tube 193. A tip like drawing 10 (B) can form the profile conic bump 103 in the electrode 2 of the IC chip 1 by using the capillary tube 193 of the above-mentioned configuration. Since a bump 103 is a profile cone form when only a dimension Z is shifted and mounted in the electrode 5 of the circuit board 4 like drawing 11 (C) in the bump 103 who formed by the above-mentioned approach, when the tip is gap to the one half of a bump's 103 outer diameter, some bumps 103 can surely contact the electrode 5 of a substrate 4. Although a part of so-called width method d of 3g of a bump's 3 plinths contacts in the conventional bump's 3 drawing 11 (D), it does not contact partially and becomes unstable junction. When this is applied to a cold energy impact test or a reflow, the amount of joint is opened. In this invention, such unstable junction is lost and junction with high production yield and dependability can be offered.

[0158] (2) According to the approach of the junction conventional example 2 of IC chip and the circuit board, connection resistance was dependent on the number of the electric conduction particles which exist between a bump and the electrode of the circuit board, but There is no need of putting an electric conduction particle between two electrodes with the above-mentioned operation gestalt of this invention for the electric flow between IC tip side electrode and a substrate lateral electrode. Without leveling a bump 3 in the leveling process as a process of having become independent A load stronger against the electrode 5 of the circuit board 4 than the conventional examples 1 and 2 Since it can push with (for example, the welding pressure of 20 or more gves per one bump 3) and a bump 3 and an electrode 5 can be joined directly, in the intervening particle number, connection resistance does not depend, is stabilized, and connection resistance is acquired. That is, in the direct junction to a bump 3 and the substrate electrode 5, the above-mentioned electric conduction particle 10a does so a contingent effect [say / that the connection resistance between the electrode 5 by the side of a substrate and the bump 3 of IC tip side can be made to fall], when electric conduction particle 10a is inserted between a bump 3 and the substrate electrode 5.

[0159] moreover, at the conventional leveling process, the bump height at the time of junction to a substrate electrode is prepared uniformly, although carried out for accumulating Since push crushing of a bump 3 can be performed to an electrode 2, or junction to 5 and coincidence with each above-mentioned operation gestalt of this invention Since it is joinable, making the curvature and wave of the circuit board 4 deform at the time of junction, and setting [the independent leveling process's being not only unnecessary, but] right

Or since it joins making the curvature and wave of the circuit board 4 deform at the time of junction, using a bump's 3,103 leveling as entirely unnecessary, and setting right by hardening the conductive paste to which the bump 3,103 was made to adhere, and making a conductive paste transform at the time of junction, it is strong to curvature or a wave.

[0160] By the way, in the conventional example 1, in 10 micrometer/IC chip (it means that the thickness curvature dimensional accuracy of 10 micrometers per IC chip is required.), and the conventional example 2, the highly precise substrate 4 and a bump 3,103 who call it 1 micrometer/IC chip (less than [bump height variation**1micrometer]) also in 2 micrometer/IC and the conventional example 3 need to be equalized, and the glass substrate represented by LCD is used in practice. On the other hand, since it joins according to the above-mentioned operation gestalt of this invention, making the curvature and wave of the circuit board 4 deform at the time of junction, and setting right, a substrate with bad flatness with curvature or a wave, for example, a resin substrate, a flexible substrate, a multilayered ceramic substrate, etc. can be used, it is more cheap and the junction approach of flexible IC chip can be offered.

[0161] Moreover, if it is made to make the volume of 6m of thermosetting resin between the IC chip 1 and the circuit board 4 larger than the volume of the space between the IC chip 1 and the circuit board 4, it can flow out so that this space may be overflowed, and the closure effectiveness can be done so. Therefore, after joining the circuit board to IC chip with the electroconductive glue needed in the conventional example 1, it is not necessary to perform closure resin (under-filling coat) to the bottom of IC chip, and a process can be shortened.

[0162] in addition, inorganic filler 6f -- 6m of thermosetting resin -- about [the] 5-90wt% -- the elastic modulus of thermosetting resin and a coefficient of thermal expansion are controllable to the optimal thing for a substrate 4 by blending. In addition, if this is used by the usual plating bump, an inorganic filler will enter between a bump and the circuit board, and junction dependability will become low. However, if a stud bump (the formation approach adapting wire bonding) is used like the above-mentioned operation gestalt of this invention By the sharp bump 3,103 who has entered into 6m of thermosetting resin at the time of junction initiation Therefore, inorganic filler 6f by pushing 6m of thermosetting resin in a bump's 3,103 direction of an outside, coming out of it, and putting Inorganic filler 6f and 6m of thermosetting resin are extruded from between a bump 3,103 and electrodes 5 and 2 in the process which the bump 3,103 deforms, it can avoid making unnecessary inclusion exist, and dependability can be raised more.

[0163] As mentioned above, according to this invention, rather than the conventional junction method of construction, productivity is good and the junction approach of cheap electronic parts, for example, IC chip, and the circuit board and its equipment can be offered.

[0164] In addition, in the above-mentioned 1st operation gestalt, it is applicable also to junction between the IC chips 1 and substrates 4 which have stud BAMBU [finishing / leveling] 300,301 as shown in drawing 37 (A) besides the bump 3 as shows drawing 1 which does not carry out leveling, and (B), respectively. In this case, although a leveling process is needed, other effectiveness, like a closure process becomes unnecessary can be done so. Moreover, the above-mentioned bump can also use the bump in whom the appearance was formed like drawing 37 (A), (B), and a profile by plating or printing. For example, a polymer bump can also be formed by forming a bump for titanium or nickel metallurgy with plating on the electrode of IC chip at this order, or printing the paste which mixed aluminum, nickel, etc. and synthetic resin on the electrode of IC chip, and drying or stiffening it. When using the bump who leveled especially, and the bump who formed by plating or printing, although there should be a possibility that it may be inserted into an inorganic filler between a bump and a substrate electrode, and the electrical installation between a bump and a substrate electrode may become unstable since it is few, a bump's deformation Electric conduction particle 10a will also be inserted between a bump and a substrate electrode, and the flow between a bump and a substrate electrode can be secured by this electric conduction particle 10a.

[0165]

[Effect of the Invention] As described above, according to this invention, many of processes conventionally taken to join the circuit board to electronic parts can be abolished, and productivity can be raised very much.

[0166] Furthermore, the following effectiveness can also be done so.

[0167] (1) It is necessary to perform the bump formation process of dedication by chip makers, and a bump's formation can be performed only by the limited manufacturer by the approach (conventional example 3) of forming a bump formation bump by plating. However, according to this invention, with wirebonding equipment, IC chip general-purpose as an example of electronic parts for wirebonding can be used, and acquisition of IC chip becomes easy.

[0168] Moreover, compared with the approach of the conventional example 1, bump leveling for stabilizing the amount of imprints of the adhesives in the unstable imprint process of the imprint of electroconductive glue becomes unnecessary, and becomes unnecessary [such leveling equipment for leveling processes].

[0169] Moreover, if a tip forms a profile conic bump in the electrode of electronic parts, since a bump is a profile cone form when a bump is shifted and mounted in the electrode of the circuit board, when the tip is gap to the one half of a bump's outer diameter, some bumps can surely contact the electrode of a substrate. Although a part of a bump's so-called plinth contacts by the conventional bump, it does not contact partially and becomes unstable junction. When this is applied to a cold energy impact test or a reflow, the amount of joint is opened. In this invention, such unstable junction is lost and junction with high production yield and dependability can be offered.

[0170] (2) According to the approach of the junction conventional example 2 of IC chip and the circuit board, connection resistance was dependent on the number of the electric conduction particles which exist between a bump and the electrode of the circuit board, but There is no need of putting an electric conduction particle between two electrodes in this invention for the electric flow between an electronic-parts lateral electrode and a substrate lateral electrode. Without leveling a bump in the leveling process as a process of having become independent A load stronger against the electrode of the circuit board than the conventional examples 1 and 2 Since it can push with (for example, the welding pressure of 20 or more gves per one bump) and a bump and an electrode can be joined directly, in the intervening particle number, connection resistance does not depend, is stabilized, and connection resistance is acquired. That is, in the direct junction to a bump and a substrate electrode, the above-mentioned electric conduction particle does so a contingent effect [say / that the connection resistance between the electrode by the side of a substrate and the bump by the side of electronic parts can be made to fall], when an electric conduction particle is inserted between a bump and a substrate electrode.

[0171] moreover, at the conventional leveling process, the bump height at the time of junction to a substrate electrode is prepared uniformly, although carried out for accumulating Since push crushing of a bump can be performed to junction to an electrode, and coincidence in this invention Since it is joinable, making the curvature and wave of the circuit board deform at the time of junction, and setting [the independent leveling process's being not only unnecessary, but] right Or since it joins making the curvature and wave of the circuit board deform at the time of junction, using a bump's leveling as entirely unnecessary, and setting right by hardening the conductive paste to which the bump was made to adhere, and making a conductive paste transform at the time of junction, it is strong to curvature or a wave.

[0172] By the way, in the conventional example 1, in 10 micrometer/IC chip (it means that the thickness curvature dimensional accuracy of 10 micrometers per IC chip is required.), and the conventional example 2, a highly precise substrate and a bump who call it 1 micrometer/IC chip (less than [bump height variation**1micrometer]) also in 2 micrometer/IC and the conventional example 3 need to be equalized, and the glass substrate represented by LCD is used in practice. On the other hand, since it is joinable according to this invention, making the curvature and wave of the circuit board deform at the time of junction, and setting right, a substrate with bad flatness with curvature or a wave, for example, a resin substrate, a flexible substrate, a multilayered ceramic substrate, etc. can be used, it is more cheap and the junction approach of flexible IC chip can be offered.

[0173] Moreover, if it is made to make the volume of the insulating resin between electronic parts and the circuit board larger than the volume of the space between electronic parts and the circuit board, it can flow out so that this space may be overflowed, and the closure effectiveness can be done so. Therefore, after joining the circuit board to IC chip with the electroconductive glue needed in the conventional example 1, it is not necessary to perform closure resin (under-filling coat) to the bottom of IC chip, and a process can be shortened.

[0174] in addition, an inorganic filler -- insulating resin -- about [the] 5-90wt% -- the elastic modulus of insulating resin and a coefficient of thermal expansion are controllable to the optimal thing for a substrate by blending. In addition, if this is used by the usual plating bump, an inorganic filler will enter between a bump and the circuit board, and junction dependability will become low. By however, the sharp bump who rubbed so that a stud bump (the formation approach adapting wire bonding) might be used like this invention, and has entered into insulating resin at ** and the time of junction initiation Therefore, an inorganic filler by pushing insulating resin in a bump's direction of an outside, coming out of it, and putting An inorganic filler and insulating resin are extruded from between a bump and electrodes in the process which the bump deforms, it can avoid making unnecessary inclusion exist, and dependability can be raised more.

[0175] moreover, in blending the inorganic filler of the same weight Use the inorganic filler in which mean

particle diameter has the mean particle diameter from which an inorganic big filler 3 micrometers or more is used, or plurality differs, or the mean particle diameter of one inorganic filler [whether the inorganic filler from which the mean particle diameter of the inorganic filler of another side differs more than twice is used, and] If one inorganic filler of at least two kinds of inorganic fillers has the mean particle diameter exceeding 3 micrometers and the inorganic filler of another side uses an inorganic filler with the mean particle diameter of 3 micrometers or less While becoming possible to be able to make the surrounding amount of moisture absorption of an inorganic filler become less, and to raise moisture resistance Can make the amount of an inorganic filler increase, and film-izing (solid state) turns easy up, and The coefficient of linear expansion of an anisotropy conductive layer, for example, an anisotropy electric conduction film sheet, or the adhesives for anisotropy electric conduction film formation can be reduced, reinforcement can be carried out more, and dependability can be raised. .

[0176] Furthermore, as for mean particle diameter, while is large, and if it is made for an inorganic filler to consist of the same ingredient as the above-mentioned insulating resin, a stress relaxation operation can be done so, and if it is softer than the epoxy resin of mean particle diameter whose inorganic filler while is large and is the above-mentioned insulating resin and above-mentioned one inorganic filler is compressed, a stress relaxation operation can be done so.

[0177] Moreover, in the junction interface of electronic parts or the above-mentioned substrate, and an anisotropy conductive layer, if an inorganic filler does not exist or the amount is lessened, the adhesive property of insulating resin original can be demonstrated, adhesive high insulating resin can increase in number in the above-mentioned junction interface, the adhesion reinforcement of electronic parts or the above-mentioned substrate, and insulating resin can be raised, and an adhesive property with electronic parts or the above-mentioned substrate will improve, with the effectiveness given of lowering the coefficient of linear expansion by the inorganic filler. Thereby, while the life in various reliability trials improves, the peel strength to bending improves.

[0178] Furthermore, in the part or layer in contact with the above-mentioned electronic parts, while using the insulating resin which raises adhesion to the film material used for an electronic-parts front face, if the insulating resin which raises adhesion to the ingredient on the front face of a substrate is used, in the part or layer in contact with the above-mentioned substrate, adhesion can be raised further. Without heating both the above-mentioned electronic parts and a substrate in both process when crushing correction and the above-mentioned bump of the curvature of the above-mentioned substrate, when impressing the above-mentioned supersonic wave and carrying out metal junction of the above-mentioned golden bump and the above-mentioned electrode of the above-mentioned substrate in each above-mentioned operation gestalt in addition, respectively After carrying out, you may make it heat [side / substrate / both / by the side of the above-mentioned electronic parts and the above-mentioned substrate] from the above-mentioned electronic-parts side.

[0179] As mentioned above, according to this invention, after joining electronic parts to the circuit board, the bump leveling process of arranging uniformly the height of the closure resin process slushed between electronic parts and a substrate or a bump is not needed, but the mounting approach of the electronic parts to the circuit board which joins electronic parts with productivity sufficient to a substrate with high-reliability, and equipment can be offered.

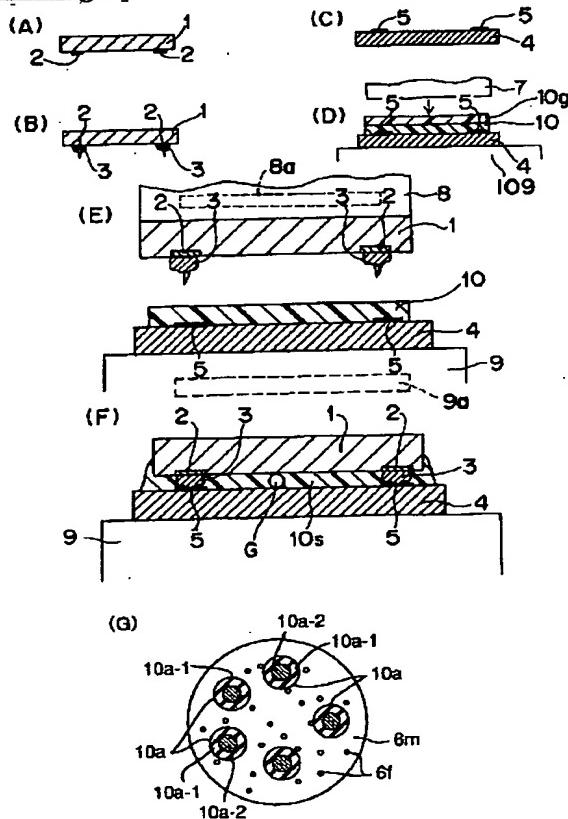
[Translation done.]

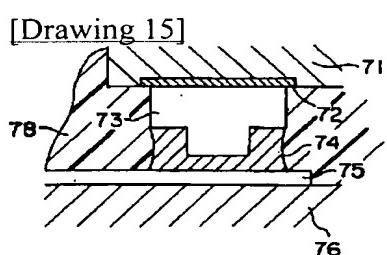
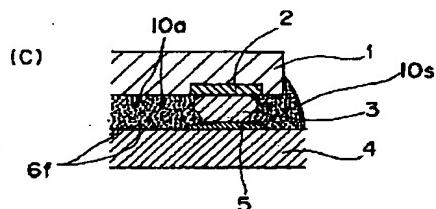
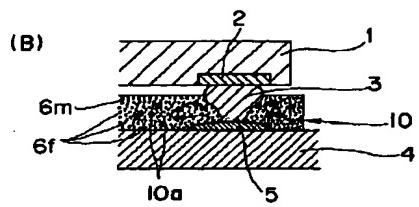
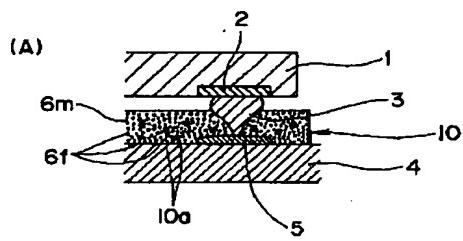
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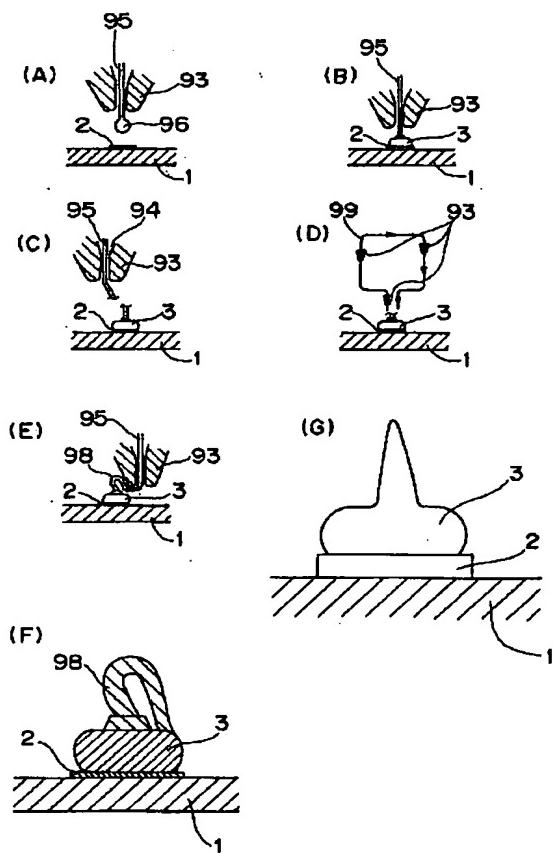
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. *** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

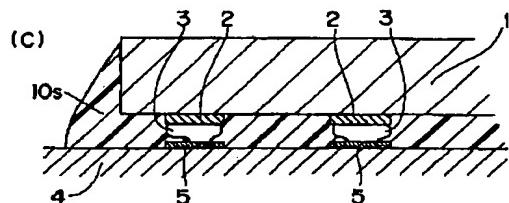
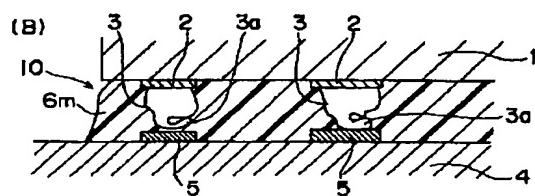
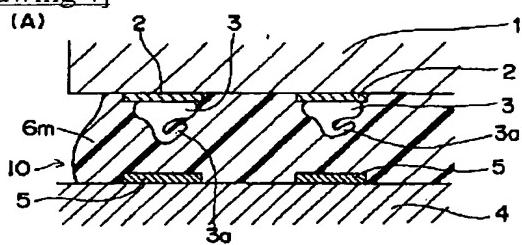
[Drawing 1][Drawing 2]



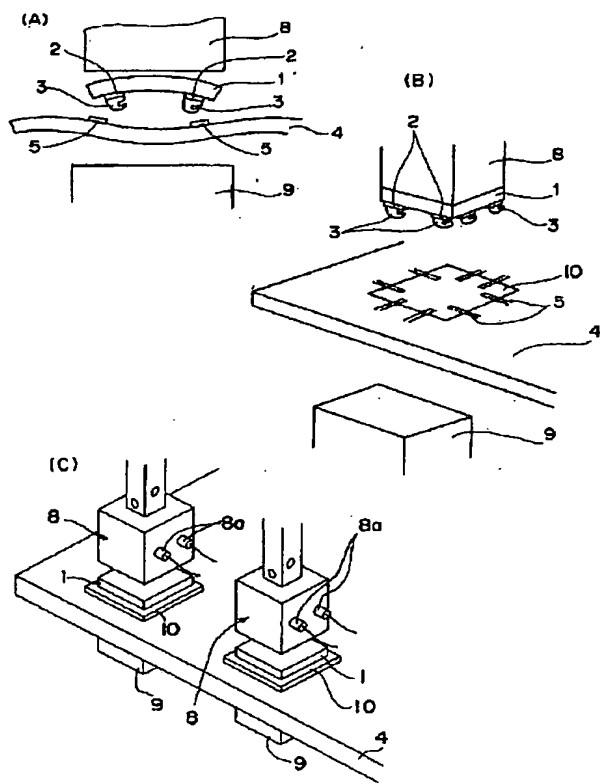
[Drawing 3]



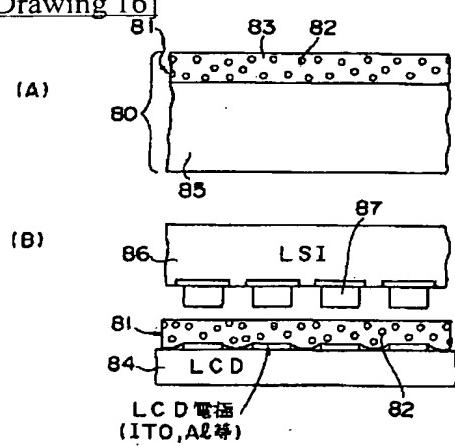
[Drawing 4]



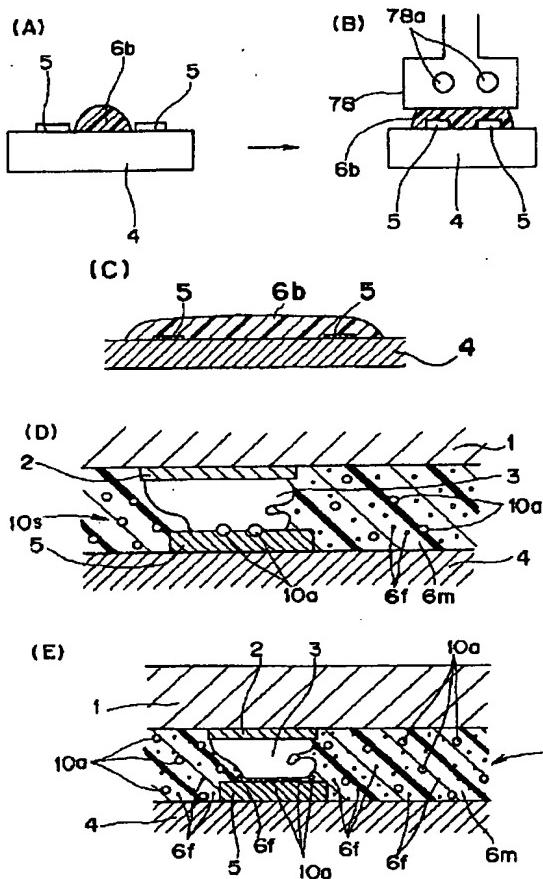
[Drawing 5]



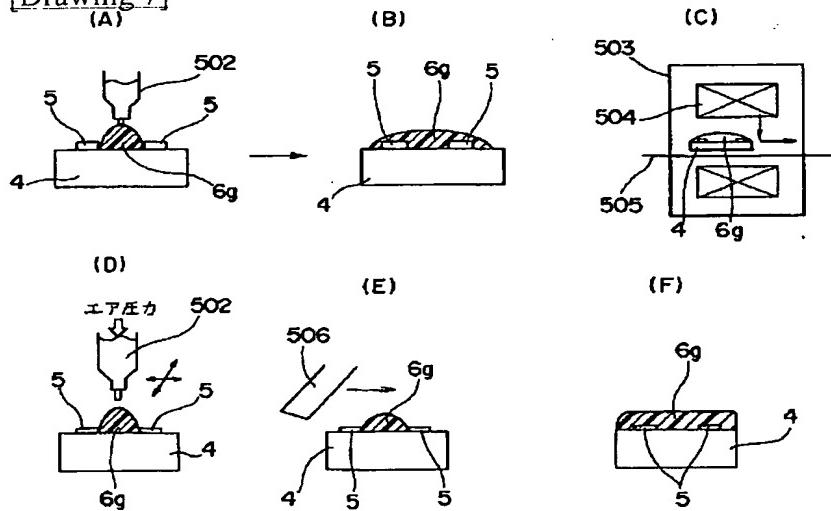
[Drawing 16]



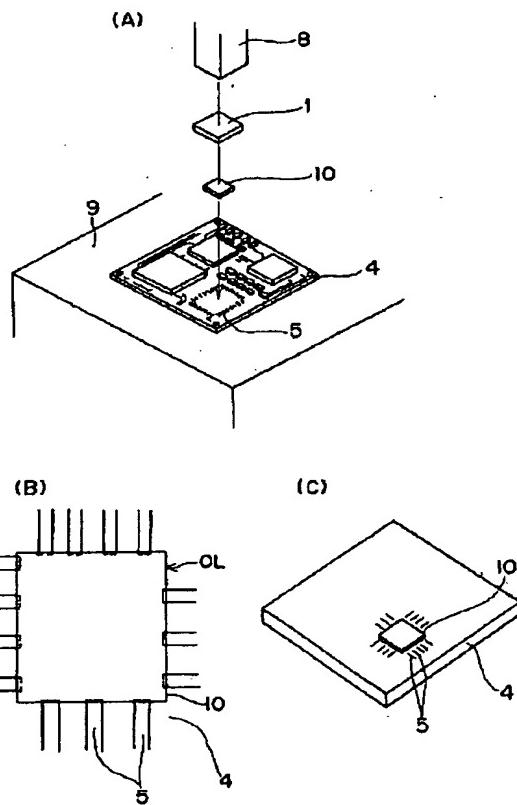
[Drawing 6]



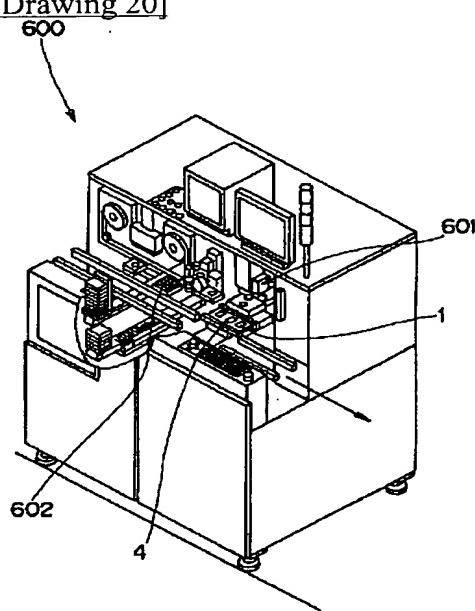
[Drawing 7]



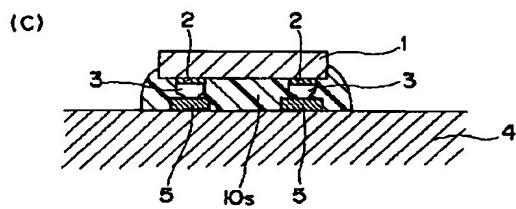
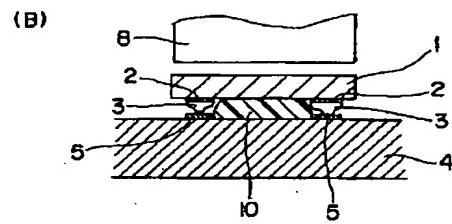
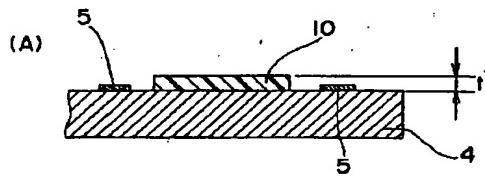
[Drawing 8]



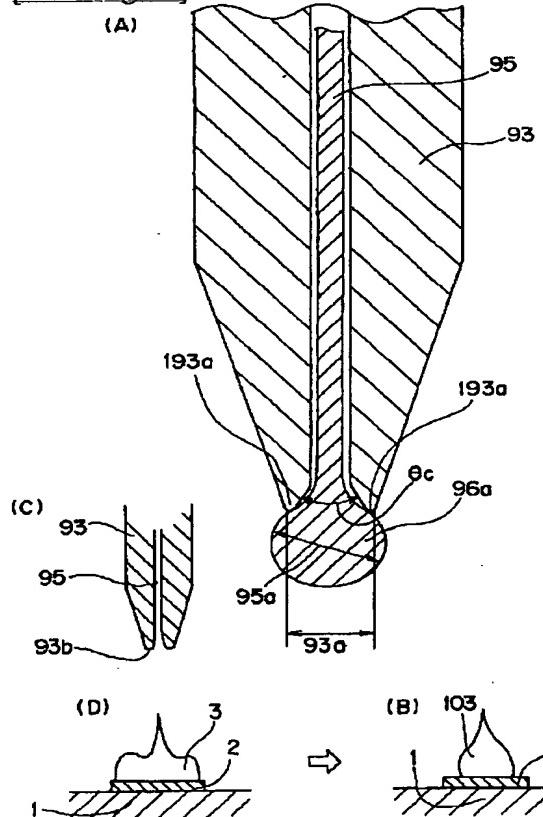
[Drawing 20]



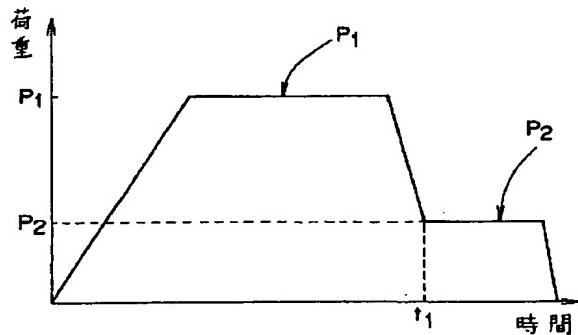
[Drawing 9]



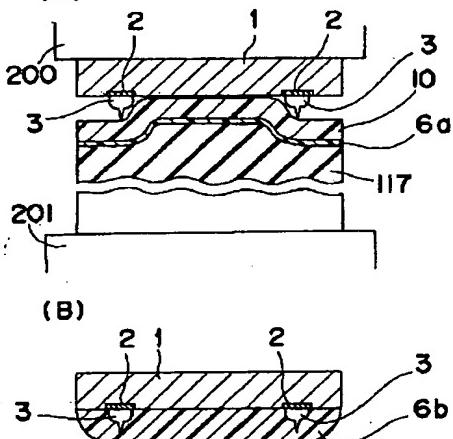
[Drawing 10]



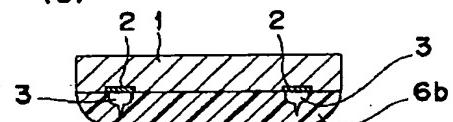
[Drawing 13]



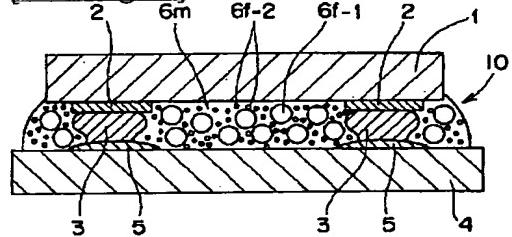
[Drawing 14]



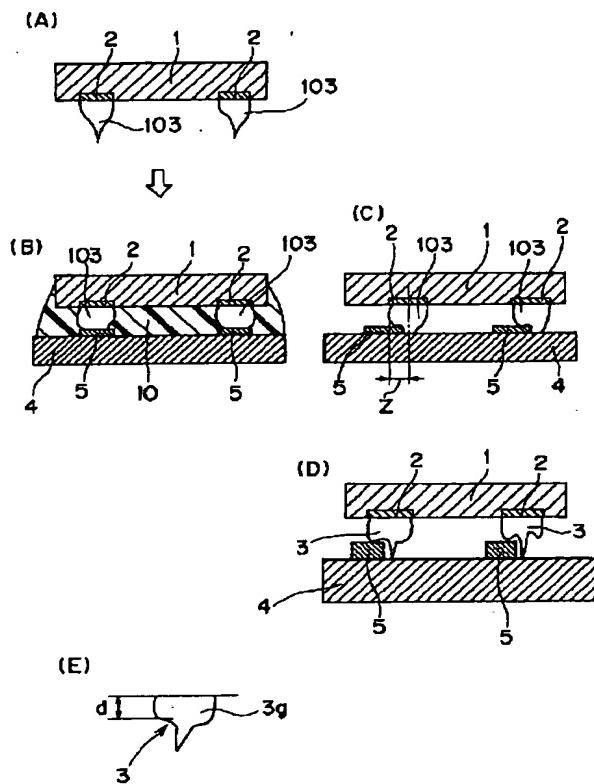
(B)



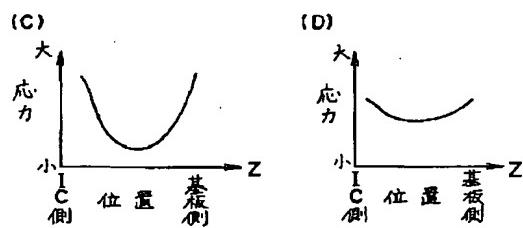
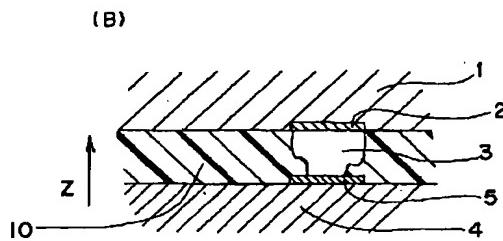
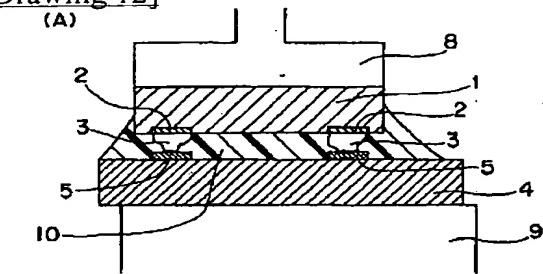
[Drawing 25]



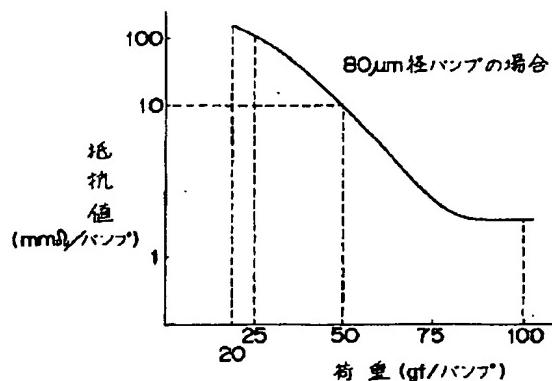
[Drawing 11]



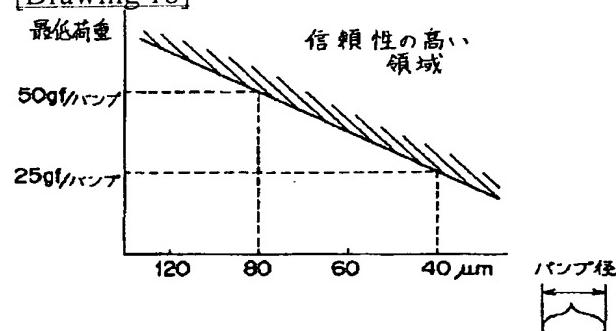
[Drawing 12]



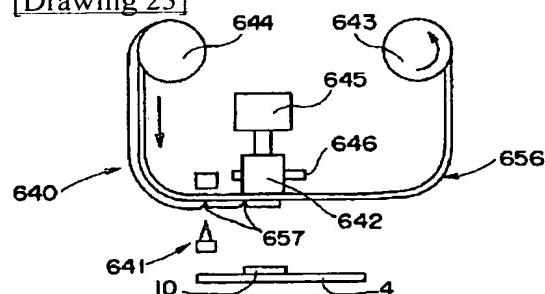
[Drawing 17]



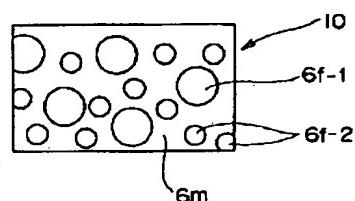
[Drawing 18]



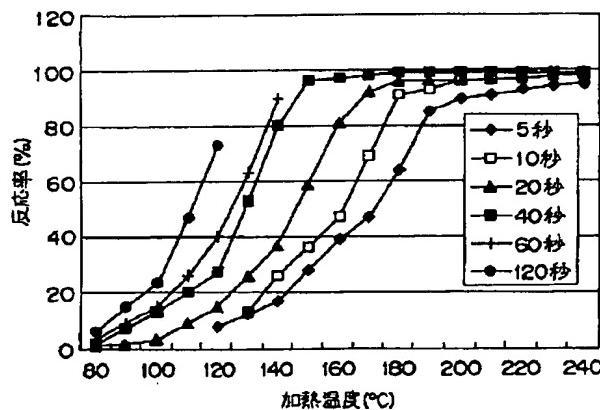
[Drawing 23]



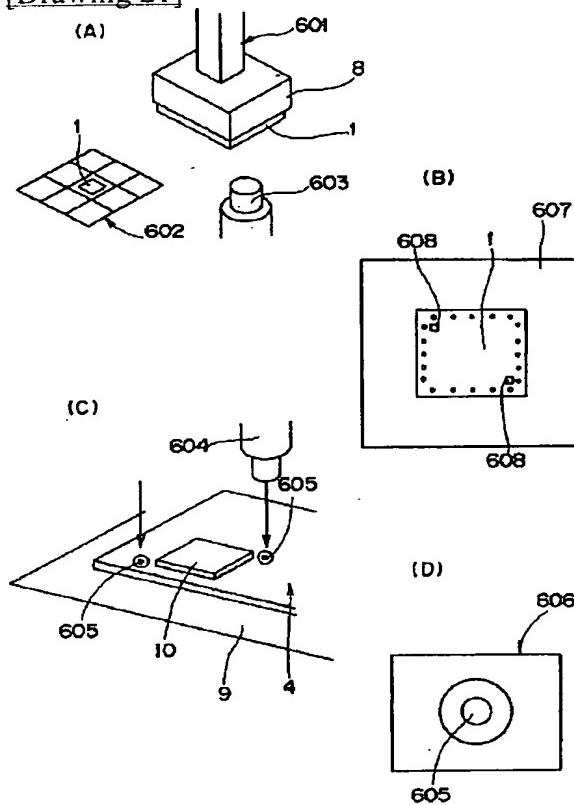
[Drawing 26]



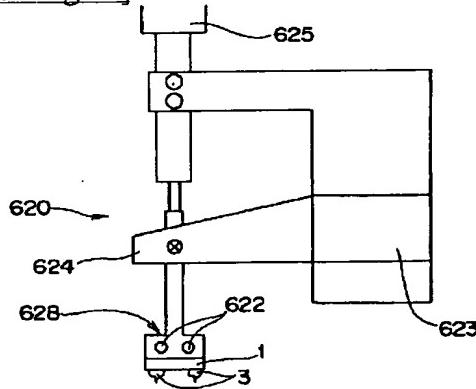
[Drawing 19]

樹脂シート反応率

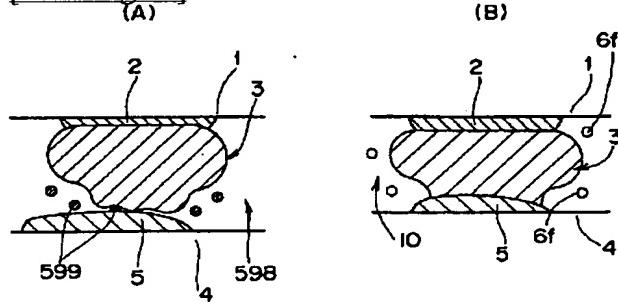
[Drawing 21]



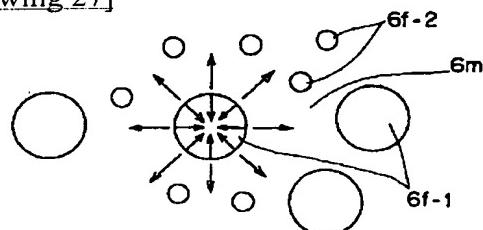
[Drawing 22]



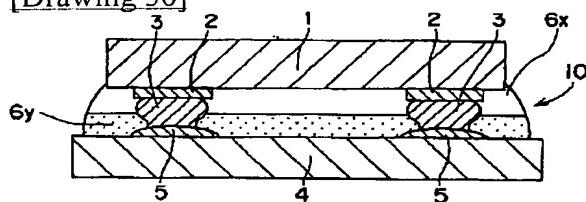
[Drawing 24]



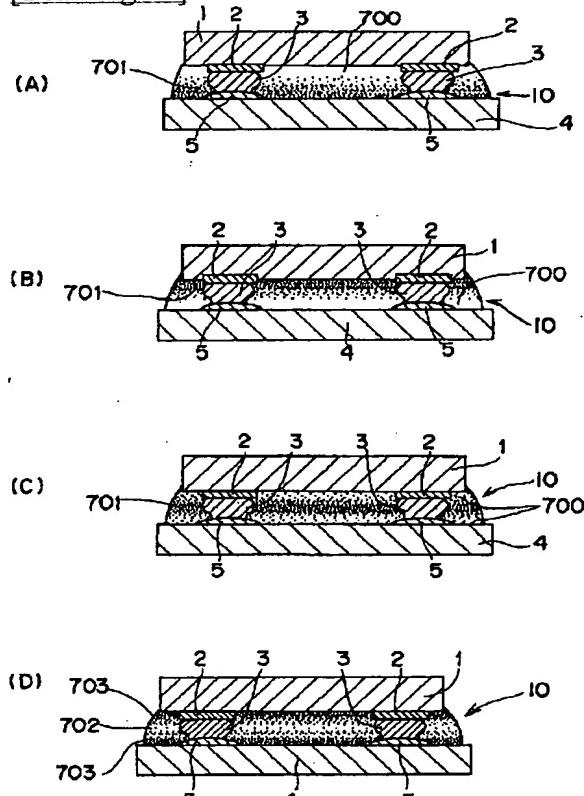
[Drawing 27]



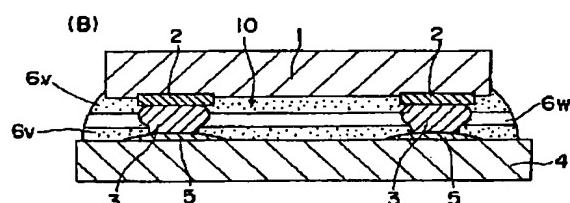
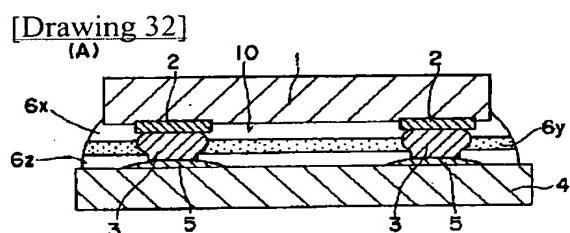
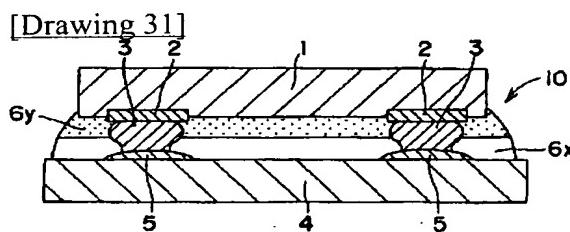
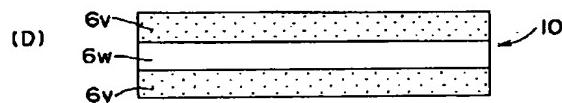
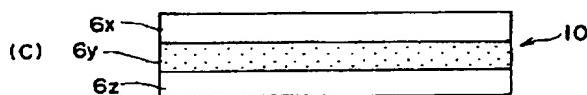
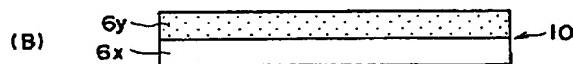
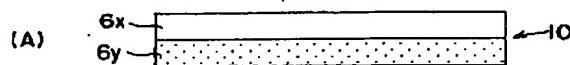
[Drawing 30]



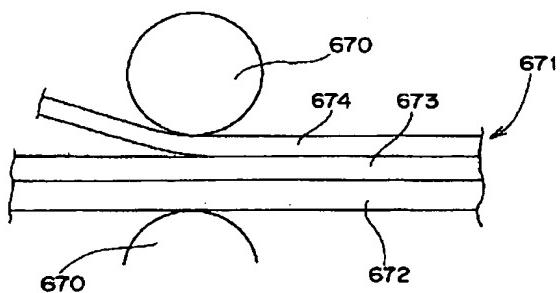
[Drawing 28]



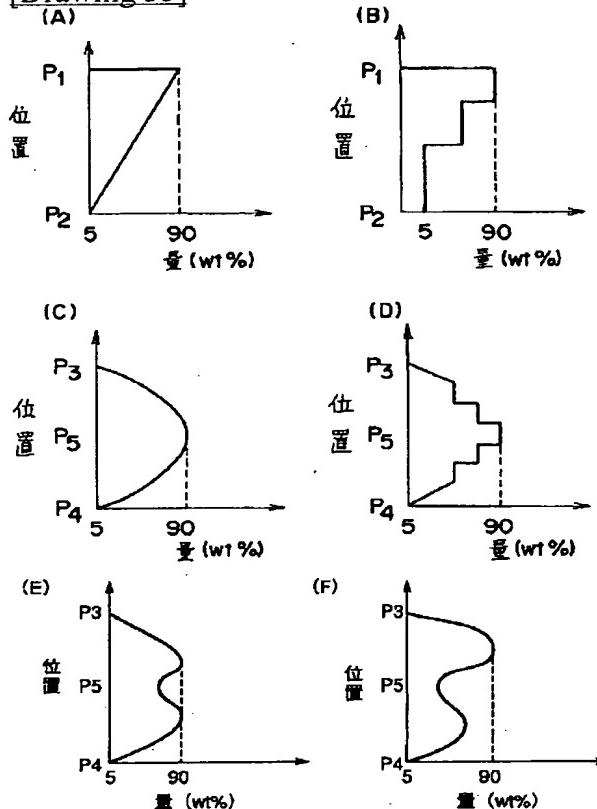
[Drawing 29]



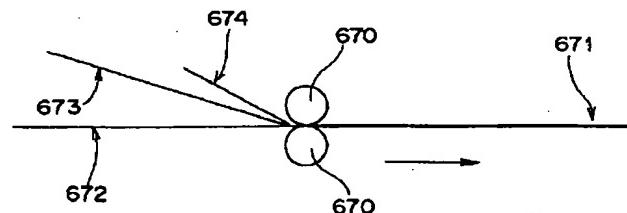
[Drawing 35]



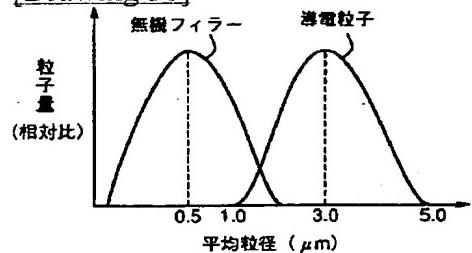
[Drawing 33]



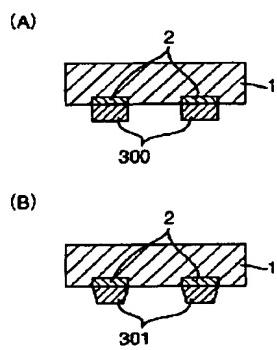
[Drawing 34]



[Drawing 36]



[Drawing 37]



[Translation done.]

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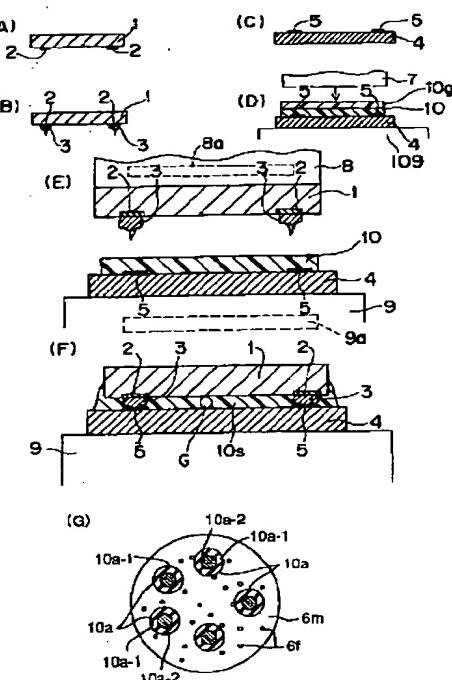
Fターム(参考) 5F044 KK02 KK04 KK07 KK21 LL09

(54) 【発明の名称】 電子部品の実装方法及びその装置

(57) 【要約】

【課題】 封止樹脂工程やバンプレベリング工程を必要とせず、導電粒子を有する異方性導電層を介在させて電子部品を基板に生産性良くかつ高信頼性で接合する電子部品実装方法及び装置を提供する。

【解決手段】 絶縁性樹脂中に導電粒子 10a と無機フィラーレ 6f を含む異方性導電層 10 を介在させつつバンプ 3 と基板電極 5 を位置合わせし、ヘッド 8 によりチップ 1 を基板 4 に 1 バンプあたり 20 gf 以上の加圧力により押圧して、チップと基板の反り矯正、バンプを押しつぶしつつ絶縁性樹脂を硬化しチップと基板を接合する。



(2)

1

【特許請求の範囲】

【請求項1】 ワイヤボンディングと同様に金属線(95)の先端に電気スパークによりボール(96, 96a)を形成し、上記形成されたボールをキャピラリー(93, 193)により電子部品(1)の電極(2)に超音波熱圧着してバンプ(3, 103)を形成し、無機フィラーを配合した絶縁性樹脂に導電粒子(10a)を配合した異方性導電層(10)を介在させながら、上記電子部品の上記電極と回路基板(4)の電極(5)とを位置合わせして上記電子部品を上記基板に搭載し、

その後、上記電子部品側から加熱しながら、又は基板側から加熱しながら、又は、上記電子部品側と上記基板側の両方から加熱しながら、ツール(8)により上記電子部品を上記回路基板に1バンプあたり20 gf以上の加圧力により押圧し、上記基板の反りの矯正と上記バンプを押しつぶしながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続するようにしたことを特徴とする電子部品の実装方法。

【請求項2】 上記バンプを形成したのち、上記異方性導電層を介在させながら、上記電子部品の上記電極と上記回路基板(4)の上記電極(5)とを位置合わせして上記電子部品を上記基板に搭載する前に、上記形成されたバンプを、一度、20 gf以下の荷重で押圧して上記バンプのネック部分の倒れを防止するように先端を整えるようにした請求項1に記載の電子部品の実装方法。

【請求項3】 上記異方性導電層の上記絶縁性樹脂(6m)が絶縁性熱硬化性エポキシ樹脂であり、この絶縁性熱硬化性エポキシ樹脂に配合する上記無機フィラーの量は上記絶縁性熱硬化性エポキシ樹脂の5~90 wt%である請求項1又は2に記載の電子部品の実装方法。

【請求項4】 上記異方性導電層の上記絶縁性樹脂(6m)は当初上記基板に塗布する際に液体であり、上記基板に塗布後、上記基板を炉(503)内に入れて上記塗布された絶縁性樹脂の液体を硬化させることにより、又は、加熱されたツール(78)により上記塗布された絶縁性樹脂の液体を押圧することにより、半固体化したのち、上記電子部品を上記基板に搭載する請求項1~3のいずれかに記載の電子部品の実装方法。

【請求項5】 ワイヤボンディングと同様に金属線(95)の先端に電気スパークによりボール(96, 96a)を形成し、上記形成されたボールをキャピラリー(93, 193)により電子部品(1)の電極(2)に超音波熱圧着して金バンプ(3, 103)を形成し、上記形成されたバンプをレベリングせずに、無機フィラーを配合した絶縁性樹脂に導電粒子(10a)を配合した異方性導電層(10)を介在させながら、上記電子部

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品の上記電極と回路基板(4)の電極(5)とを位置合わせして上記電子部品を上記基板に搭載し、その後、ツール(8)により上記電子部品の上面側から荷重を印加して上記金バンプのネック部分の倒れを防止するように先端を整えるとともに超音波を印加して上記金バンプと上記基板の上記電極とを金属接合し、次に、上記電子部品の上記上面側から加熱しながら、又は、上記基板側から加熱しながら、又は、上記電子部品側と上記基板側の両方から加熱しながら、上記電子部品を上記回路基板に1バンプあたり20 gf以上の加圧力により押圧し、上記基板の反りの矯正と上記バンプを押しつぶしながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続するようにしたことを特徴とする電子部品の実装方法。

【請求項6】 上記電子部品(1)は複数の電極(2)を有し、上記位置合わせの前に、上記回路基板(4)に、上記異方性導電層として、上記電子部品(1)の上記複数の電極(2)を結んだ外形寸法(OL)より小さい形状寸法の固形の異方性導電膜シート(10)を貼り付けたのち上記位置合わせを行い、上記接合においては、上記異方性導電膜シート(10)を加熱しながら、上記電子部品を上記回路基板に加圧押圧して、上記回路基板の反りの矯正を同時に進行しながら、上記電子部品と上記回路基板の間に介在する上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合するようにした請求項1~5のいずれかに記載の電子部品の実装方法。

【請求項7】 上記バンプを上記電子部品上に形成する際にワイヤボンディングと同様に金属線(95)の先端に電気スパークにより金ボール(96a)を形成するとき、チャムファ一角(θ_c)を100°以下とし、かつ、上記金ボールと接する部分に平らな部位を設けない先端形状を有する上記キャピラリーにより、先端が大略円錐状の上記金バンプを上記電子部品の上記電極に形成する請求項1~6のいずれかに記載の電子部品の実装方法。

【請求項8】 ワイヤボンディングと同様に金属線(95)の先端に電気スパークによりボール(96, 96a)を形成し、上記形成されたボールをキャピラリー(93, 193)により電子部品(1)の電極(2)にバンプ(3, 103)を形成し、上記形成されたバンプをレベリングせずに、無機フィラーを配合した絶縁性樹脂に導電粒子(10a)を配合した異方性導電層(10)を介在させながら、上記電子部品の上記電極と回路基板(4)の電極(5)とを位置合わせして上記電子部品を上記基板に搭載し、その後、所定温度に加熱されたツール(8)により上記電子部品の上面から加熱しながら、加圧力として上記電子部品を上記回路基板に圧力P1により押圧して上記基

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板の反りの矯正を行いながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化し、その後、所定時間後、上記加圧力を上記圧力P1より低い圧力P2に降下させて上記異方性導電層の上記絶縁性樹脂の硬化時の応力を緩和しながら、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続するようにしたことを特徴とする電子部品の実装方法。

【請求項9】 上記圧力P1は20gf／バンプ以上、上記圧力P2は上記圧力P1の1／2以下とする請求項8に記載の電子部品の実装方法。

【請求項10】 無機フィラーを配合した絶縁性樹脂に導電粒子(10a)を配合した異方性導電層(10)を、回路基板(4)の電極(5)又は電子部品(1)に貼り付ける装置(7, 109, 200, 201)と、上記電子部品(1)の電極(2)にワイヤボンディングと同様に金属線(95)の先端に電気スパークによりボール(96, 96a)を形成し、これをキャピラリー(93, 193)により上記基板の上記電極に超音波熱圧着して形成してレベリングしないバンプ(3, 103)を形成する装置(93, 193)と、上記電子部品を上記回路基板(4)の上記電極(5)に位置合わせて搭載する装置(600)と、ツール(8)により、加熱しながら、上記電子部品を上記回路基板に1バンプあたり20gf以上の加圧力により押圧し、上記基板の反りの矯正を行いながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続する装置(8, 9)とを備えるようにしたことを特徴とする電子部品の実装装置。

【請求項11】 上記異方性導電層の上記絶縁性樹脂が絶縁性熱硬化性エポキシ樹脂であり、この絶縁性熱硬化性エポキシ樹脂に配合する上記無機フィラーの量は上記絶縁性熱硬化性エポキシ樹脂の5～90wt%である請求項10に記載の電子部品の実装装置。

【請求項12】 上記異方性導電層の上記絶縁性樹脂(6m)は液体であり、上記絶縁性樹脂の液体を上記基板に塗布するディスペンサ(502)と、該ディスペンサにより上記基板に塗布された上記絶縁性樹脂の液体を、上記塗布された基板を挿入して硬化させて上記絶縁性樹脂を半固体化する炉(503)とを備えるようにした請求項10又は11に記載の電子部品の実装装置。

【請求項13】 上記異方性導電層の上記絶縁性樹脂(6m)は液体であり、上記絶縁性樹脂の液体を上記基板に塗布するディスペンサ(502)と、該ディスペンサにより上記基板に塗布された上記絶縁性樹脂の液体を押圧して上記絶縁性樹脂を半固体化する裝

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置(78)とを備える請求項10又は11に記載の電子部品の実装装置。

【請求項14】 無機フィラーを配合した絶縁性樹脂に導電粒子(10a)を配合した異方性導電層(10)を、回路基板(4)の電極(5)又は電子部品(1)に貼り付ける装置(7, 109, 200, 201)と、上記電子部品(1)の電極(2)にワイヤボンディングと同様に金属線(95)の先端に電気スパークによりボール(96, 96a)を形成し、これをキャピラリー(93, 193)により上記基板の上記電極に超音波熱圧着して形成してレベリングしない金バンプ(3, 103)を形成する装置(93, 193)と、上記電子部品を上記回路基板(4)の上記電極(5)に位置合わせて搭載する装置(600)と、ツール(628)により上記電子部品の上面から荷重を印加して上記金バンプのネック部分の倒れを防止するよう先端を整えるとともに超音波を印加して上記金バンプと上記基板の上記電極とを金属接合する装置(620)と、

ツール(8)により加熱しながら、上記電子部品を上記回路基板に1バンプあたり20gf以上の加圧力により押圧し、上記基板の反りの矯正を行うとともに上記バンプを押しつぶしながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続する装置(8, 9)とを備えるようにしたことを特徴とする電子部品の実装装置。

【請求項15】 上記位置合わせの前に、上記回路基板(4)に、上記異方性導電層として、上記電子部品(1)の電極(2)を結んだ外形寸法(OL)より小さい形状寸法の固形の異方性導電膜シート(10)を貼り付ける装置(640)と、

この後、上記回路基板と電子部品の位置合わせを行い装着する装置(600)と、接合においては、上記異方性導電膜シート(10)を加熱しながら、上記電子部品を上記回路基板に加圧押圧して、上記回路基板の反りの矯正を同時に進行しながら、上記電子部品と上記回路基板の間に介在する上記異方性導電膜シートを硬化して、上記電子部品と上記回路基板を接合する装置(7, 8)を具備する請求項10～13のいずれかに記載の電子部品の実装装置。

【請求項16】 上記金ボール(96a)を形成する装置(93, 193)は、上記金ボールと接する部分に平らな部位を設けない先端形状を有するとともにチャムファーア一角(θc)が100°以下となる上記キャピラリーを有して、該キャピラリーにより、先端が大略円錐状の上記金バンプを上記電子部品の上記電極に形成する請求項10～15のいずれかに記載の電子部品の実装装置。

【請求項17】 無機フィラーを配合した絶縁性樹脂に

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導電粒子(10a)を配合した異方性導電層(10)を回路基板(4)又は電子部品(1)に貼り付ける装置

(7, 109, 200, 201)と、

上記電子部品(1)の電極(2)にワイヤボンディング同様に金属線(95)の先端に電気スパークによりボール(96, 96a)を形成し、これをキャビラリー(93, 193)により上記基板の上記電極に形成してレベリングしないバンプ(3, 103)を形成する装置(93, 193)と、

上記電子部品を上記回路基板(4)の上記電極(5)に位置合わせて搭載する装置(600)と、

所定温度に加熱されたツール(8)により、上記電子部品の上面から加熱しながら、加圧力として上記電子部品を上記回路基板に圧力P1により押圧して上記基板の反りの矯正を行いながら、上記電子部品と上記回路基板の間に介在する上記絶縁性樹脂を硬化し、その後、所定時間後、上記加圧力を上記圧力P1より低い圧力P2に降下させて上記異方性導電層の上記絶縁性樹脂の硬化時の応力を緩和しながら上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続する装置(8, 9)とを備えるようにしたことを特徴とする電子部品の実装装置。

【請求項18】 上記圧力P1は20g f／バンプ以上、上記圧力P2は上記圧力P1の1/2以下とする請求項17に記載の電子部品の実装装置。

【請求項19】 上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーの平均粒径が3μm以上であることを特徴とする請求項1～3のいずれかに記載の電子部品の実装方法。

【請求項20】 上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、異なる平均粒径を持つ複数種類の無機フィラー(6f-1, 6f-2)である請求項1～3, 19のいずれかに記載の電子部品の実装方法。

【請求項21】 上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー(6f-1, 6f-2)であって、上記少なくとも2種類の無機フィラーのうちの一方の無機フィラー(6f-1)の平均粒径は、上記少なくとも2種類の無機フィラーのうちの他方の無機フィラー(6f-2)の平均粒径の2倍以上異なる請求項1～3, 19のいずれかに記載の電子部品の実装方法。

【請求項22】 上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー(6f-1, 6f-2)であって、上記少なくとも2種類の無機フィラーのうちの一方の無機フィラー(6f-1)は3μmを超える平均粒径を持ち、上記少なくとも2種類の無機フィラーのうちの他方の無機フィラー(6f-2)は3μm

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以下の平均粒径を持つ請求項1～3, 19のいずれかに記載の電子部品の実装方法。

【請求項23】 上記異方性導電層の上記絶縁性樹脂(6m)に配合する上記無機フィラー(6f)は、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー(6f-1, 6f-2)であって、上記少なくとも2種類の無機フィラーのうちの平均粒径の大きい一方の無機フィラー(6f-1)は上記絶縁性樹脂と同一材料からなることにより、応力緩和作用を奏する請求項1～3, 19のいずれかに記載の電子部品の実装方法。

【請求項24】 上記異方性導電層の上記絶縁性樹脂(6m)に配合する上記無機フィラー(6f)は、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー(6f-1, 6f-2)であって、上記少なくとも2種類の無機フィラーのうちの平均粒径の大きい一方の無機フィラー(6f-1)は上記絶縁性樹脂(6m)であるエポキシ樹脂よりも柔らかく、上記一方の無機フィラー(6f-1)が圧縮されることにより、応力緩和作用を奏する請求項1～3, 19のいずれかに記載の電子部品の実装方法。

【請求項25】 上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分が、他の部分よりも上記無機フィラー量が少ないようにした請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項26】 上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分に位置されかつ上記絶縁性樹脂と同一の絶縁性樹脂に上記無機フィラーを配合した第1樹脂層(6x)と、上記第1樹脂層に接觸し、かつ、上記第1樹脂層よりも上記無機フィラー量が少ない絶縁性樹脂で構成される第2樹脂層(6y)とを備える請求項25に記載の電子部品の実装方法。

【請求項27】 上記異方性導電層は、上記電子部品及び上記基板にそれぞれ接觸する部分が、他の部分よりも上記無機フィラー量が少ないようにした請求項25に記載の電子部品の実装方法。

【請求項28】 上記異方性導電層は、上記第1樹脂層の上記第2樹脂層とは反対側に、上記第1樹脂層よりも上記無機フィラー量が少ない絶縁性樹脂で構成される第3樹脂層(6z)をさらに備えて、上記第1樹脂層と上記第3樹脂層は、それぞれ、上記電子部品と上記基板に接觸する請求項26に記載の電子部品の実装方法。

【請求項29】 上記電子部品及び上記基板にそれぞれ接觸する部分は、その上記無機フィラー量が20wt%未満にする一方、上記他の部分はその上記無機フィラー量が20wt%以上である請求項27に記載の電子部品の実装方法。

【請求項30】 上記第1樹脂層及び上記第3樹脂層のそれぞれは、その上記無機フィラー量が20wt%未満にする一方、上記第2樹脂層はその上記無機フィラー量

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が20wt%以上である請求項28に記載の電子部品の実装方法。

【請求項31】 上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分から他の部分に向かって、上記無機フィラー量が徐々に又は段階的に少なくなるようにした請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項32】 上記異方性導電層は、上記電子部品及び上記基板にそれぞれ接触する部分から他の部分に向かって、上記無機フィラー量が徐々に又は段階的に少くなるようにした請求項31に記載の電子部品の実装方法。

【請求項33】 上記電子部品に接触する部分では、電子部品表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を用いる一方、上記基板に接触する部分では、基板表面の材料に対して密着性を向上させる絶縁性樹脂を用いるようにした請求項25, 27, 29, 31のいずれかに記載の電子部品の実装方法。

【請求項34】 上記電子部品に接触する上記樹脂層では、電子部品表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を用いる一方、上記基板に接触する上記樹脂層では、基板表面の材料に対して密着性を向上させる絶縁性樹脂を用いるようにした請求項26, 28, 30, 32のいずれかに記載の電子部品の実装方法。

【請求項35】 上記異方性導電層(10)は、上記電子部品又は上記基板のいずれか一方に接触する部分が、上記無機フィラーを配合しないようにした請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項36】 上記異方性導電層(10)は、上記電子部品又は上記基板のいずれか一方に接触する部分に位置されかつ上記絶縁性樹脂と同一の絶縁性樹脂に上記無機フィラーを配合した第1樹脂層(6x)と、上記第1樹脂層に接触し、かつ、上記無機フィラーを配合しない絶縁性樹脂で構成される第2樹脂層(6y)とを備える請求項35に記載の電子部品の実装方法。

【請求項37】 上記異方性導電層(10)は、上記電子部品及び上記基板にそれぞれ接触する部分が、上記無機フィラーを配合しないようにした請求項35に記載の電子部品の実装方法。

【請求項38】 上記異方性導電層(10)は、上記第1樹脂層の上記第2樹脂層とは反対側に、上記無機フィラーを配合しない絶縁性樹脂で構成される第3樹脂層(6z)をさらに備えて、上記第1樹脂層と上記第3樹脂層は、それぞれ、上記電子部品と上記基板に接触する請求項36に記載の電子部品の実装方法。

【請求項39】 上記電子部品及び上記基板にそれぞれ接触する部分は、上記無機フィラーを配合しないようする一方、上記他の部分はその上記無機フィラー量が2

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0wt%以上である請求項37に記載の電子部品の実装方法。

【請求項40】 上記第1樹脂層及び上記第3樹脂層のそれぞれは、上記無機フィラーを配合しないようする一方、上記第2樹脂層はその上記無機フィラー量が20wt%以上である請求項38に記載の電子部品の実装方法。

【請求項41】 上記異方性導電層(10)は、上記電子部品及び上記基板に接触する部分に位置されかつ上記無機フィラーを配合した絶縁性樹脂で構成される第4樹脂層(6v)と、上記電子部品と上記基板との中間部分に位置されかつ上記第4樹脂層よりも上記無機フィラー量が少ない絶縁性樹脂で構成される第5樹脂層(6w)とを備える請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項42】 上記異方性導電層(10)は、上記電子部品及び上記基板に接触する部分に位置されかつ上記無機フィラーを配合した絶縁性樹脂で構成される第4樹脂層(6v)と、上記電子部品と上記基板との中間部分に位置されかつ上記無機フィラー量が含まれていない絶縁性樹脂で構成される第5樹脂層(6w)とを備える請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項43】 上記異方性導電層(10)は、上記電子部品及び上記基板にそれぞれ接触する部分から、上記電子部品及び上記基板との中間部分に向かって、上記無機フィラー量が徐々に少なくなるようにした請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項44】 上記異方性導電層(10)は、上記電子部品の近傍部分、次いで、上記基板の近傍部分、次いで、上記電子部品の近傍部分と上記基板の近傍部分との中間部分の順に上記無機フィラー量が少ないようにした請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

【請求項45】 上記異方性導電層(10)の上記電子部品の近傍部分と上記基板の近傍部分とのそれぞれの無機フィラー量は、上記電子部品の上記異方性導電層に接触する部分の線膨張係数と上記基板の上記異方性導電層に接触する部分の線膨張係数とにそれぞれ対応して配合されるようにした請求項43又は44に記載の電子部品の実装方法。

【請求項46】 電子部品(1)の電極(2)に形成されたバンプ(3, 103)を、絶縁性樹脂(6m)に無機フィラー(6f)が配合されかつ硬化された異方性導電層(10)を介在させかつ上記バンプが押しつぶされた状態で、回路基板(4)の電極(5)に接合されて上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続しており、

【請求項47】 上記異方性導電層(10)は、上記電子部品又は上記基板に接触する部分に位置されかつ上記無機フィラーを配合した絶縁性樹脂で構成される第4樹脂層(6v)と、上記電子部品と上記基板との中間部分に位置されかつ上記第4樹脂層よりも上記無機フィラー量が少ない絶縁性樹脂で構成される第5樹脂層(6w)とを備える請求項1～3, 19～24のいずれかに記載の電子部品の実装方法。

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板のいずれか一方に接触する部分が、他の部分よりも上記無機フィラー量が少ないようにしたことを特徴とする電子部品ユニット。

【請求項47】 電子部品(1)の電極(2)に形成されたバンプ(3, 103)を、絶縁性樹脂(6m)に無機フィラー(6f)が配合されかつ硬化された異方性導電層(10)を介在させかつ上記バンプが押しつぶされた状態で、回路基板(4)の電極(5)に接合されて上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続しており、上記異方性導電層(10)は、上記電子部品又は上記基板のいずれか一方に接触する部分に位置されかつ上記絶縁性樹脂と同一の絶縁性樹脂に上記無機フィラーを配合した第1樹脂層(6x)と、上記第1樹脂層に接触し、かつ、上記第1樹脂層よりも上記無機フィラー量が少ない絶縁性樹脂で構成される第2樹脂層(6y)とを備えるようにしたことを特徴とする電子部品ユニット。

【請求項48】 上記超音波を印加して上記金バンプと上記基板の上記電極とを金属接合するとき、上記電子部品の上記上面側から加熱しながら、又は、上記基板側から加熱しながら、又は、上記電子部品側と上記基板側の両方から加熱するようにした請求項5に記載の電子部品の実装方法。

【請求項49】 請求項1～9, 19～45, 48のいずれかに記載の電子部品の実装方法により上記電子部品が上記基板に実装された電子部品ユニット。

【請求項50】 上記バンプはめつき又は印刷により形成したバンプである請求項1～9, 19～45のいずれかに記載の電子部品の実装方法。

【請求項51】 上記バンプはめつき又は印刷により形成したバンプである請求項46～49のいずれかに記載の電子部品ユニット。

【請求項52】 上記異方性導電層は、上記無機フィラーを配合した固形の絶縁性樹脂に、上記無機フィラーの平均粒径より大きい平均直径を有する導電粒子(10a)を配合した請求項1～9, 19～45, 50のいずれかに記載の電子部品の実装方法。

【請求項53】 上記異方性導電層は、上記無機フィラー(6f)を配合した固形の絶縁性樹脂に、上記無機フィラーの平均粒径がより大きい平均直径を有する導電粒子(10a)を配合した請求項10～18のいずれかに記載の電子部品の実装装置。

【請求項54】 上記異方性導電層は、上記無機フィラー(6f)を配合した固形の絶縁性樹脂に、上記無機フィラーの平均粒径がより大きい平均直径を有する導電粒子(10a)を配合した請求項46～49, 51のいずれかに記載の電子部品ユニット。

【請求項55】 上記超音波を印加して上記金バンプと上記基板の上記電極とを金属接合する装置は、上記電子部品の上記上面側から、又は、上記基板側から、又は、

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上記電子部品側と上記基板側の両方から加熱する加熱部材を備えて、上記金属接合時に上記加熱部材により加熱するようにした請求項14に記載の電子部品の実装装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、電子回路用プリント基板(本明細書では、代表例として「基板」と称するが、この「基板」にはインタポーラや電子部品が装着される他の部品などの被装着体を意味する。)に電子部品例えばICチップや表面弹性波(SAW)デバイスなどを単体(ICチップの場合にはペアIC)状態で実装する回路基板への電子部品の実装方法及びその装置及び上記実装方法により上記電子部品が上記基板に実装された電子部品ユニットに関するものである。

【0002】

【従来の技術】今日、電子回路基板は、あらゆる製品に使用されるようになり、日増しにその性能が向上し、回路基板上で用いられる周波数も高くなっている。インピーダンスが低くなるフリップチップ実装は高周波を使用する電子機器に適した実装方法となっている。また、携帯機器の増加から、回路基板にICチップをパッケージではなく裸のまま搭載するフリップチップ実装が求められている。このために、ICチップそのまま単体で回路基板に搭載したときのICチップや、電子機器及びフラットパネルディスプレイへ実装したICチップには、一定数の不良品が混在している。また、上記フリップチップ以外にもCSP(Chip Size Package)、BGA(Ball Grid Array)等が用いられるようになってきている。

【0003】従来の電子機器の回路基板へICチップを接合する方法(従来例1)としては特公平06-66355号公報等により開示されたものがある。これを図15に示す。図15に示すように、バンプ73を形成したICチップ71にAgペースト74を転写して回路基板76の電極75に接続したのちAgペースト74を硬化し、その後、封止材78をICチップ71と回路基板76の間に流し込む方法が一般的に知られている。

【0004】また、液晶ディスプレイにICチップを接合する方法(従来例2)として、図16に示される特公昭62-6652号公報のように、異方性導電フィルム80を使用するものであって、絶縁性樹脂83中に導電性微片82を加えて構成する異方性導電接着剤層81をセパレータ85から剥がして基板や液晶ディスプレイ84のガラスに塗布し、ICチップ86を熱圧着することによって、Auバンプ87の下以外のICチップ86の下面と基板84の間に上記異方性導電接着剤層81が介在している半導体チップの接続構造が、一般に知られている。

【0005】従来例3としては、UV硬化樹脂を基板に

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塗布し、その上にICチップをマウントし加圧しながら、UV照射することにより両者の間の樹脂を硬化し、その収縮力により両者間のコンタクトを維持する方法が、知られている。

【0006】このように、ICチップを接合するには、フラットパッケージのようなICチップをリードフレーム上にダイボンディングし、ICチップの電極とリードフレームをワイヤボンドしてつなぎ、樹脂成形してパッケージを形成した後に、クリームハンダを回路基板に印刷し、その上にフラットパッケージICを搭載しリフローするという工程を行うことにより、上記接合が行われていた。これらのSMT(Surface Mount

Technology)といわれる工法では、ICをパッケージにする工程が長く、IC部品の生産に時間を要し、また、回路基板を小型化するのが困難であった。例えばICチップは、フラットパックに封止された状態では、ICチップの約4～10倍程度の面積を必要とするため、小型化を妨げる要因となっていた。

【0007】これに対し、工程の短縮と小型軽量化の為にICチップを裸の状態でダイレクトに基板に搭載するフリップチップ工法が最近では用いられるようになってきた。このフリップチップ工法は、ICチップへのバンプ形成、バンプレベリング、Ag·Pdペースト転写、実装、検査、封止樹脂による封止、検査とを行うスタンド・バンプ・ボンディング(SBB)や、ICチップへのバンプ形成と基板へのUV硬化樹脂塗布とを並行して行い、その後、実装、樹脂のUV硬化、検査を行うUV樹脂接合のような多くの工法が開発されている。

【0008】

【発明が解決しようとする課題】ところが、どの工法においてもICチップのバンプと基板の電極を接合するペーストの硬化や封止樹脂の塗布硬化に時間がかかり生産性が悪いという欠点を有していた。また、回路基板として、反り量を管理されたセラミックやガラスを用いる必要があり、高価となる欠点を有していた。

【0009】また、従来例1のような導電性ペーストを接合材に用いる工法においては、その転写量を安定化するために、ICチップのバンプはレベリングして、平坦化してから用いる必要があった。

【0010】また、従来例2のような異方性導電接着剤による接合構造においては、回路基板の基材としてガラスを用いるものが開発されているが、ICチップ側電極と基板側電極との間の電気的導通のために導電粒子を両電極間に挟み込む必要があるため、導電性接着剤中の導電粒子を均一に分散することが必要となるが、導電性接着剤中の導電粒子を均一に分散することが困難であり、粒子の分散異常によりショートの原因になったり、導電性接着剤が高価であったり、バンプの高さをそろえる為に、ICチップの電極のバンプは電気メッキにより形成しなければならなかったりした。

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【0011】また、従来例3のようにUV硬化樹脂を用いて接合する方法においては、バンプの高さバラツキを±1(μm)以下にしなければならず、また、樹脂基板(ガラスエポキシ基板)等の平面度の悪い基板には接合することができないといった問題があった。また、ハンダを用いる方法においても、接合後に基板とICチップの熱膨張収縮差を緩和する為に封止樹脂を流し込み硬化する必要があった。この樹脂封止の硬化には、2～8時間の時間を必要とし、生産性がきわめて悪いといった問題があった。

【0012】従って、本発明の目的は、上記問題を解決することにあって、回路基板と電子部品を接合した後に、電子部品と基板の間に流し込む封止樹脂工程やバンプの高さを一定に揃えるバンプレベリング工程を必要とせず、導電粒子を有する異方性導電層を介在させて電子部品を基板に生産性良くかつ高信頼性で接合する回路基板への電子部品の実装方法及び装置及び上記実装方法により上記電子部品が上記基板に実装された電子部品ユニットを提供することにある。

【0013】

【課題を解決するための手段】上記目的を達成するため、本発明は以下のように構成する。

【0014】本発明の第1態様によれば、ワイヤボンディングと同様に金属線の先端に電気スパークによりボールを形成し、上記形成されたボールをキャピラーにより電子部品の電極に超音波熱圧着してバンプを形成し、無機フィラーを配合した絶縁性樹脂に導電粒子を配合した異方性導電層を介在させながら、上記電子部品の上記電極と回路基板の電極とを位置合わせて上記電子部品を上記基板に搭載し、その後、上記電子部品側から加熱しながら、又は基板側から加熱しながら、又は、上記電子部品側と上記基板側の両方から加熱しながら、ツールにより上記電子部品を上記回路基板に1バンプあたり20gf以上の加压力により押圧し、上記基板の反りの矯正と上記バンプを押しつぶしながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続するようにしたことを特徴とする電子部品の実装方法を提供する。

【0015】本発明の第2態様によれば、上記バンプを形成したのち、上記異方性導電層を介在させながら、上記電子部品の上記電極と上記回路基板の上記電極とを位置合わせて上記電子部品を上記基板に搭載する前に、上記形成されたバンプを、一度、20gf以下の荷重で押圧して上記バンプのネック部分の倒れを防止するよう先端を整えるようにした第1態様に記載の電子部品の実装方法を提供する。

【0016】本発明の第3態様によれば、上記異方性導電層の上記絶縁性樹脂が絶縁性熱硬化性エポキシ樹脂で

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あり、この絶縁性熱硬化性エポキシ樹脂に配合する上記無機フィラーの量は上記絶縁性熱硬化性エポキシ樹脂の5～90wt%である第1又は2態様に記載の電子部品の実装方法を提供する。

【0017】本発明の第4態様によれば、上記異方性導電層の上記絶縁性樹脂は当初上記基板に塗布する際に液体であり、上記基板に塗布後、上記基板を炉内に入れて上記塗布された絶縁性樹脂の液体を硬化させることにより、又は、加熱されたツールにより上記塗布された絶縁性樹脂の液体を押圧することにより、半固体化したのち、上記電子部品を上記基板に搭載する第1～3のいずれかの態様に記載の電子部品の実装方法を提供する。

【0018】本発明の第5態様によれば、ワイヤボンディングと同様に金属線の先端に電気スパークによりボールを形成し、上記形成されたボールをキャピラリーにより電子部品の電極に超音波熱圧着して金パンプを形成し、上記形成されたパンプをレベリングせずに、無機フィラーを配合した絶縁性樹脂に導電粒子を配合した異方性導電層を介在させながら、上記電子部品の上記電極と回路基板の電極とを位置合わせて上記電子部品を上記基板に搭載し、その後、ツールにより上記電子部品の上面側から荷重を印加して上記金パンプのネック部分の倒れを防止するように先端を整えるとともに超音波を印加して上記金パンプと上記基板の上記電極とを金属接合し、次に、上記電子部品の上記上面側から加熱しながら、又は、上記基板側から加熱しながら、又は、上記電子部品側と上記基板側の両方から加熱しながら、上記電子部品を上記回路基板に1パンプあたり20gf以上の加压力により押圧し、上記基板の反りの矯正と上記パンプを押しつぶしながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続するようにしたことを特徴とする電子部品の実装方法を提供する。

【0019】本発明の第6態様によれば、上記電子部品は複数の電極を有し、上記位置合わせの前に、上記回路基板に、上記異方性導電層として、上記電子部品の上記複数の電極を結んだ外形寸法より小さい形状寸法の固形の異方性導電膜シートを貼り付けたのち上記位置合わせを行い、上記接合においては、上記異方性導電膜シートを加熱しながら、上記電子部品を上記回路基板に加圧押圧して、上記回路基板の反りの矯正を同時に進行しながら、上記電子部品と上記回路基板の間に介在する上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合するようにした第1～5のいずれかの態様に記載の電子部品の実装方法を提供する。

【0020】本発明の第7態様によれば、上記パンプを上記電子部品上に形成する際にワイヤボンディングと同様に金属線の先端に電気スパークにより金ボールを形成

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するとき、チャムファー一角を100°以下とし、かつ、上記金ボールと接する部分に平らな部位を設けない先端形状を有する上記キャピラリーにより、先端が大略円錐状の上記金パンプを上記電子部品の上記電極に形成する第1～6のいずれかの態様に記載の電子部品の実装方法を提供する。

【0021】本発明の第8態様によれば、ワイヤボンディングと同様に金属線の先端に電気スパークによりボールを形成し、上記形成されたボールをキャピラリーにより電子部品の電極にパンプを形成し、上記形成されたパンプをレベリングせずに、無機フィラーを配合した絶縁性樹脂に導電粒子を配合した異方性導電層を介在させながら、上記電子部品の上記電極と回路基板の電極とを位置合わせて上記電子部品を上記基板に搭載し、その後、所定温度に加熱されたツールにより上記電子部品の上面から加熱しながら、加圧力として上記電子部品を上記回路基板に圧力P1により押圧して上記基板の反りの矯正を行なながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化し、その後、所定時間後、上記加圧力を上記圧力P1より低い圧力P2に降下させて上記異方性導電層の上記絶縁性樹脂の硬化時の応力を緩和しながら、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続するようにしたことを特徴とする電子部品の実装方法を提供する。

【0022】本発明の第9態様によれば、上記圧力P1は20gf/パンプ以上、上記圧力P2は上記圧力P1の1/2以下とする第8態様に記載の電子部品の実装方法を提供する。

【0023】本発明の第10態様によれば、無機フィラーを配合した絶縁性樹脂に導電粒子を配合した異方性導電層を、回路基板の電極又は電子部品に貼り付ける装置と、上記電子部品の電極にワイヤボンディングと同様に金属線の先端に電気スパークによりボールを形成し、これをキャピラリーにより上記基板の上記電極に超音波熱圧着して形成してレベリングしないパンプを形成する装置と、上記電子部品を上記回路基板の上記電極に位置合わせて搭載する装置と、ツールにより、加熱しながら、上記電子部品を上記回路基板に1パンプあたり20gf以上の加圧力により押圧し、上記基板の反りの矯正を行なながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続する装置とを備えるようにしたことを特徴とする電子部品の実装装置を提供する。

【0024】本発明の第11態様によれば、上記異方性導電層の上記絶縁性樹脂が絶縁性熱硬化性エポキシ樹脂であり、この絶縁性熱硬化性エポキシ樹脂に配合する上記無機フィラーの量は上記絶縁性熱硬化性エポキシ樹脂

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の5～90wt%である第10態様に記載の電子部品の実装装置を提供する。

【0025】本発明の第12態様によれば、上記異方性導電層の上記絶縁性樹脂は液体であり、上記絶縁性樹脂の液体を上記基板に塗布するディスペンサと、該ディスペンサにより上記基板に塗布された上記絶縁性樹脂の液体を、上記塗布された基板を挿入して硬化させて上記絶縁性樹脂を半固体化する炉とを備えるようにした第10又は11態様に記載の電子部品の実装装置を提供する。

【0026】本発明の第13態様によれば、上記異方性導電層の上記絶縁性樹脂は液体であり、上記絶縁性樹脂の液体を上記基板に塗布するディスペンサと、該ディスペンサにより上記基板に塗布された上記絶縁性樹脂の液体を押圧して上記絶縁性樹脂を半固体化する装置とを備える第10又は11態様に記載の電子部品の実装装置を提供する。

【0027】本発明の第14態様によれば、無機フィラーを配合した絶縁性樹脂に導電粒子を配合した異方性導電層を、回路基板の電極又は電子部品に貼り付ける装置と、上記電子部品の電極にワイヤボンディングと同様に金属線の先端に電気スパークによりボールを形成し、これをキャピラリーにより上記基板の上記電極に超音波熱圧着して形成してレベリングしない金パンプを形成する装置と、上記電子部品を上記回路基板の上記電極に位置合わせして搭載する装置と、ツールにより上記電子部品の上面から荷重を印加して上記金パンプのネック部分の倒れを防止するように先端を整えるとともに超音波を印加して上記金パンプと上記基板の上記電極とを金属接合する装置と、ツールにより加熱しながら、上記電子部品を上記回路基板に1パンプあたり20gf以上の加圧力により押圧し、上記基板の反りの矯正を行うとともに上記パンプを押しつぶしながら、上記電子部品と上記回路基板の間に介在する上記異方性導電層の上記絶縁性樹脂を硬化して、上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続する装置とを備えるようにしたことを特徴とする電子部品の実装装置を提供する。

【0028】本発明の第15態様によれば、上記位置合わせの前に、上記回路基板に、上記異方性導電層として、上記電子部品の電極を結んだ外形寸法より小さい形状寸法の固形の異方性導電膜シートを貼り付ける装置と、この後、上記回路基板と電子部品の位置合わせを行い装着する装置と、接合においては、上記異方性導電膜シートを加熱しながら、上記電子部品を上記回路基板に加压押圧して、上記回路基板の反りの矯正を同時にいながら、上記電子部品と上記回路基板の間に介在する上記異方性導電膜シートを硬化して、上記電子部品と上記回路基板を接合する装置を具備する第10～13のいずれかの態様に記載の電子部品の実装装置を提供する。

【0029】本発明の第16態様によれば、上記金ボーラーを形成する装置は、上記金ボールと接する部分に平らな部位を設けない先端形状を有するとともにチャムファ一角が100°以下となる上記キャピラリーを有して、該キャピラリーにより、先端が大略円錐状の上記金パンプを上記電子部品の上記電極に形成する第10～15のいずれかの態様に記載の電子部品の実装装置を提供する。

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【0030】本発明の第17態様によれば、無機フィラーを配合した絶縁性樹脂に導電粒子を配合した異方性導電層を回路基板又は電子部品に貼り付ける装置と、上記電子部品の電極にワイヤボンディング同様に金属線の先端に電気スパークによりボールを形成し、これをキャピラリーにより上記基板の上記電極に形成してレベリングしないパンプを形成する装置と、上記電子部品を上記回路基板の上記電極に位置合わせして搭載する装置と、所定温度に加熱されたツールにより、上記電子部品の上面から加熱しながら、加圧力として上記電子部品を上記回路基板に圧力P1により押圧して上記基板の反りの矯正を行なながら、上記電子部品と上記回路基板の間に介在する上記絶縁性樹脂を硬化し、その後、所定時間後、上記加圧力を上記圧力P1より低い圧力P2に降下させて上記異方性導電層の上記絶縁性樹脂の硬化時の応力を緩和しながら上記電子部品と上記回路基板を接合して上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続する装置とを備えるようにしたことを特徴とする電子部品の実装装置を提供する。

【0031】本発明の第18態様によれば、上記圧力P1は20gf／パンプ以上、上記圧力P2は上記圧力P1の1/2以下とする第17態様に記載の電子部品の実装装置を提供する。

【0032】本発明の第19態様によれば、上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーの平均粒径が3μm以上であることを特徴とする第1～3のいずれかの態様に記載の電子部品の実装方法を提供する。

【0033】本発明の第20態様によれば、上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、異なる平均粒径を持つ複数種類の無機フィラーである第1～3、19のいずれかの態様に記載の電子部品の実装方法を提供する。

【0034】本発明の第21態様によれば、上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラーであって、上記少なくとも2種類の無機フィラーのうちの一方の無機フィラーの平均粒径は、上記少なくとも2種類の無機フィラーのうちの他方の無機フィラーの平均粒径の2倍以上異なっている第1～3、19のいずれかの態様に記載の電子部品の実装方法を提供する。

【0035】本発明の第22態様によれば、上記異方性

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導電層の上記絶縁性樹脂に配合する上記無機フィラーは、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラーであって、上記少なくとも2種類の無機フィラーのうちの一方の無機フィラーは $3\text{ }\mu\text{m}$ を超える平均粒径を持ち、上記少なくとも2種類の無機フィラーのうちの他方の無機フィラーは $3\text{ }\mu\text{m}$ 以下の平均粒径を持つ第1～3、19のいずれかの態様に記載の電子部品の実装方法を提供する。

【0036】本発明の第23態様によれば、上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラーであって、上記少なくとも2種類の無機フィラーのうちの平均粒径の大きい一方の無機フィラーは上記絶縁性樹脂と同一材料からなることにより、応力緩和作用を奏する第1～3、19のいずれかの態様に記載の電子部品の実装方法を提供する。

【0037】本発明の第24態様によれば、上記異方性導電層の上記絶縁性樹脂に配合する上記無機フィラーは、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラーであって、上記少なくとも2種類の無機フィラーのうちの平均粒径の大きい一方の無機フィラーは上記絶縁性樹脂であるエポキシ樹脂よりも柔らかく、上記一方の無機フィラーが圧縮されることにより、応力緩和作用を奏する第1～3、19のいずれかの態様に記載の電子部品の実装方法を提供する。

【0038】本発明の第25態様によれば、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分が、他の部分よりも上記無機フィラーラー量が少ないようとした第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0039】本発明の第26態様によれば、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分に位置されかつ上記絶縁性樹脂と同一の絶縁性樹脂に上記無機フィラーを配合した第1樹脂層と、上記第1樹脂層に接触し、かつ、上記第1樹脂層よりも上記無機フィラーラー量が少ない絶縁性樹脂で構成される第2樹脂層とを備える第25態様に記載の電子部品の実装方法を提供する。

【0040】本発明の第27態様によれば、上記異方性導電層は、上記電子部品及び上記基板にそれぞれ接触する部分が、他の部分よりも上記無機フィラーラー量が少ないようとした第25態様に記載の電子部品の実装方法を提供する。

【0041】本発明の第28態様によれば、上記異方性導電層は、上記第1樹脂層の上記第2樹脂層とは反対側に、上記第1樹脂層よりも上記無機フィラーラー量が少ない絶縁性樹脂で構成される第3樹脂層をさらに備えて、上記第1樹脂層と上記第3樹脂層は、それぞれ、上記電子部品と上記基板に接触する第26態様に記載の電子部品の実装方法を提供する。

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【0042】本発明の第29態様によれば、上記電子部品及び上記基板にそれぞれ接触する部分は、その上記無機フィラーラー量が 20 wt\% 未満にする一方、上記他の部分はその上記無機フィラーラー量が 20 wt\% 以上である第27態様に記載の電子部品の実装方法を提供する。

【0043】本発明の第30態様によれば、上記第1樹脂層及び上記第3樹脂層のそれぞれは、その上記無機フィラーラー量が 20 wt\% 未満にする一方、上記第2樹脂層はその上記無機フィラーラー量が 20 wt\% 以上である第28態様に記載の電子部品の実装方法を提供する。

【0044】本発明の第31態様によれば、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分から他の部分に向かって、上記無機フィラーラー量が徐々に又は段階的に少くなるようにした第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0045】本発明の第32態様によれば、上記異方性導電層は、上記電子部品及び上記基板にそれぞれ接触する部分から他の部分に向かって、上記無機フィラーラー量が徐々に又は段階的に少くなるようにした第31態様に記載の電子部品の実装方法を提供する。

【0046】本発明の第33態様によれば、上記電子部品に接触する部分では、電子部品表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を用いる一方、上記基板に接触する部分では、基板表面の材料に対して密着性を向上させる絶縁性樹脂を用いるようにした第25、27、29、31のいずれかの態様に記載の電子部品の実装方法を提供する。

【0047】本発明の第34態様によれば、上記電子部品に接触する上記樹脂層では、電子部品表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を用いる一方、上記基板に接触する上記樹脂層では、基板表面の材料に対して密着性を向上させる絶縁性樹脂を用いるようにした第26、28、30、32のいずれかの態様に記載の電子部品の実装方法を提供する。

【0048】本発明の第35態様によれば、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分が、上記無機フィラーラーを配合しないようにした第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0049】本発明の第36態様によれば、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接触する部分に位置されかつ上記絶縁性樹脂と同一の絶縁性樹脂に上記無機フィラーラーを配合した第1樹脂層と、上記第1樹脂層に接触し、かつ、上記無機フィラーラーを配合しない絶縁性樹脂で構成される第2樹脂層とを備える第35態様に記載の電子部品の実装方法を提供する。

【0050】本発明の第37態様によれば、上記異方性導電層は、上記電子部品及び上記基板にそれぞれ接触する部分が、上記無機フィラーラーを配合しないようにした第

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35 様様に記載の電子部品の実装方法を提供する。

【0051】本発明の第38態様によれば、上記異方性導電層は、上記第1樹脂層の上記第2樹脂層とは反対側に、上記無機フィラーを配合しない絶縁性樹脂で構成される第3樹脂層をさらに備えて、上記第1樹脂層と上記第3樹脂層は、それぞれ、上記電子部品と上記基板に接觸する第36態様に記載の電子部品の実装方法を提供する。

【0052】本発明の第39態様によれば、上記電子部品及び上記基板にそれぞれ接觸する部分は、上記無機フィラーを配合しないようにする一方、上記他の部分はその上記無機フィラーラー量が20wt%以上である第37態様に記載の電子部品の実装方法を提供する。

【0053】本発明の第40態様によれば、上記第1樹脂層及び上記第3樹脂層のそれぞれは、上記無機フィラーを配合しないようにする一方、上記第2樹脂層はその上記無機フィラーラー量が20wt%以上である第38態様に記載の電子部品の実装方法を提供する。

【0054】本発明の第41態様によれば、上記異方性導電層は、上記電子部品及び上記基板に接觸する部分に位置されかつ上記無機フィラーを配合した絶縁性樹脂で構成される第4樹脂層と、上記電子部品と上記基板との中間部分に位置されかつ上記第4樹脂層よりも上記無機フィラーラー量が少ない絶縁性樹脂で構成される第5樹脂層とを備える第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0055】本発明の第42態様によれば、上記異方性導電層は、上記電子部品及び上記基板に接觸する部分に位置されかつ上記無機フィラーを配合した絶縁性樹脂で構成される第4樹脂層と、上記電子部品と上記基板との中間部分に位置されかつ上記無機フィラーラー量が含まれていない絶縁性樹脂で構成される第5樹脂層とを備える第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0056】本発明の第43態様によれば、上記異方性導電層は、上記電子部品及び上記基板にそれぞれ接觸する部分から、上記電子部品及び上記基板との中間部分に向かって、上記無機フィラーラー量が徐々に少なくなるようにした第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0057】本発明の第44態様によれば、上記異方性導電層は、上記電子部品の近傍部分、次いで、上記基板の近傍部分、次いで、上記電子部品の近傍部分と上記基板の近傍部分との中間部分の順に上記無機フィラーラー量が少なくなった第1～3、19～24のいずれかの態様に記載の電子部品の実装方法を提供する。

【0058】本発明の第45態様によれば、上記異方性導電層の上記電子部品の近傍部分と上記基板の近傍部分とのそれぞれの無機フィラーラー量は、上記電子部品の上記異方性導電層に接觸する部分の線膨張係数と上記基板の

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上記異方性導電層に接觸する部分の線膨張係数とにそれぞれ対応して配合されたようにした第43又は44態様に記載の電子部品の実装方法を提供する。

【0059】本発明の第46態様によれば、電子部品の電極に形成されたパンプを、絶縁性樹脂に無機フィラーが配合されかつ硬化された異方性導電層を介在させかつ上記パンプが押しつぶされた状態で、回路基板の電極に接合されて上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続しており、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接觸する部分が、他の部分よりも上記無機フィラーラー量が少ないようにしたことを特徴とする電子部品ユニットを提供する。

【0060】本発明の第47態様によれば、電子部品の電極に形成されたパンプを、絶縁性樹脂に無機フィラーが配合されかつ硬化された異方性導電層を介在させかつ上記パンプが押しつぶされた状態で、回路基板の電極に接合されて上記電子部品の上記電極と上記回路基板の上記電極を電気的に接続しており、上記異方性導電層は、上記電子部品又は上記基板のいずれか一方に接觸する部分に位置されかつ上記絶縁性樹脂と同一の絶縁性樹脂に上記無機フィラーラーを配合した第1樹脂層と、上記第1樹脂層に接觸し、かつ、上記第1樹脂層よりも上記無機フィラーラー量が少ない絶縁性樹脂で構成される第2樹脂層とを備えるようにしたことを特徴とする電子部品ユニットを提供する。

【0061】本発明の第48態様によれば、上記超音波を印加して上記金パンプと上記基板の上記電極とを金属接合するとき、上記電子部品の上記上面側から加熱しながら、又は、上記基板側から加熱しながら、又は、上記電子部品側と上記基板側の両方から加熱するようにした第5の態様に記載の電子部品の実装方法を提供する。本発明の第49態様によれば、第1～9、19～45、48のいずれかの態様に記載の電子部品の実装方法により上記電子部品が上記基板に実装された電子部品ユニットを提供する。

【0062】本発明の第50態様によれば、上記パンプはめっき又は印刷により形成したパンプである第1～9、19～45のいずれかの態様に記載の電子部品の実装方法を提供する。

【0063】本発明の第51態様によれば、上記パンプはめっき又は印刷により形成したパンプである第46～49のいずれかの態様に記載の電子部品ユニットを提供する。

【0064】本発明の第52態様によれば、上記異方性導電層は、上記無機フィラーラーを配合した固形の絶縁性樹脂に、上記無機フィラーラーの平均粒径より大きい平均直徑を有する導電粒子を配合した第1～9、19～45、50のいずれかの態様に記載の電子部品の実装方法を提供する。

【0065】本発明の第53態様によれば、上記異方性

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導電層は、上記無機フィラーを配合した固形の絶縁性樹脂に、上記無機フィラーの平均粒径がより大きい平均直径を有する導電粒子を配合した第10～18のいずれかの態様に記載の電子部品の実装装置を提供する。

【0066】本発明の第54態様によれば、上記異方性導電層は、上記無機フィラーを配合した固形の絶縁性樹脂に、上記無機フィラーの平均粒径がより大きい平均直径を有する導電粒子を配合した第46～49、51のいずれかの態様に記載の電子部品ユニットを提供する。本発明の第55態様によれば、上記超音波を印加して上記金パンプと上記基板の上記電極とを金属接合する装置は、上記電子部品の上記上面側から、又は、上記基板側から、又は、上記電子部品側と上記基板側の両方から加熱する加熱部材を備えて、上記金属接合時に上記加熱部材により加熱するようにした第14の態様に記載の電子部品の実装装置を提供する。

【0067】

【発明の実施の形態】以下に、本発明にかかる実施の形態を図面に基づいて詳細に説明する。

【0068】(第1実施形態)以下、本発明の第1実施形態にかかる電子部品の実装方法及びその装置の一例としての回路基板へのICチップの実装方法及びその実装装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えば半導体装置を図1(A)から図14を参照しながら説明する。

【0069】まず、本発明の第1実施形態にかかる回路基板へのICチップ実装方法を図1(A)～図4(C)及び図6(A)～(F)を用いて説明する。

【0070】図1(A)の電子部品の一例であるICチップ1においてICチップ1のA1パッド電極2にワイヤボンディング装置により図3(A)～図3(F)のごとき動作によりパンプ(突起電極)3を形成する。すなわち、図3(A)でホルダであるキャピラリー93から突出したワイヤ95の下端にポール96を形成し、図3(B)でワイヤ95を保持するキャピラリー93を下降させ、ポール96をICチップ1の電極2に接合して大略パンプ3の形状を形成し、図3(C)でワイヤ95を下方に送りつつキャピラリー93の上昇を開始し、図3(D)に示すような大略矩形のループ99にキャピラリー93を移動させて図3(E)に示すようにパンプ3の上部に湾曲部98を形成し、引きちぎることにより図1(B)、図3(F)に示すようなパンプ3を形成する。あるいは、図3(B)でワイヤ95をキャピラリー93でクランプして、キャピラリー93を上昇させて上方に引き上げることにより、金属線、例えば、金ワイヤ(金線)95(なお、金属線の例としては、スズ、アルミニウム、銅、又はこれらの金属に微量元素を含有させた合金のワイヤなどがあるが、以下の実施形態では代表例として金ワイヤ(金線)として記載する。)を引きちぎ

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り、図3(G)のようなパンプ3の形状を形成するようにもよい。このように、ICチップ1の各電極2にパンプ3を形成した状態を図1(B)に示す。

【0071】次いで、この実施形態では、各電極2にパンプ3が形成されたICチップ1を回路基板4へ装着するとき、異方性導電層の一例として、異方性導電膜(ACF)シート10を介在させるものである。この異方性導電膜シート10は、異方性導電膜シート10を構成する絶縁性熱硬化性の固形樹脂中の導電粒子10aの平均直径より小さい平均直径の無機フィラー6fを含有する。例えば、図36に示すように、導電粒子10aの平均直径を、従来のACFでの導電粒子10aの平均直径1.0μmより小さい0.5μmとするとき、無機フィラー6fの粒子の平均直径は3～5μm程度とする。異方性導電膜シート10に含まれる上記導電粒子10aとして、ニッケル粉に金メッキを施したもの用いる。このように構成することにより、基板側の電極5とICチップ側のパンプ3との間での接続抵抗値を低下せしめることができて尚好適である。

【0072】上記導電粒子10aとしては、さらに好ましくは、上記導電粒子10aの導電粒子本体10a-1の外側に絶縁層10a-2でコートしたものを用い、導電粒子10aの量を通常汎用されている異方性導電膜の2倍以上とすることにより、ある確率でパンプ3に導電粒子10aが挟まれることになり、吸湿時の膨潤やその後のリフローによる熱衝撃に対する耐性を向上することができる。

【0073】このように絶縁コートされた導電粒子10aは、パンプ3で基板電極5との間に挟み込まれると、そのときに導電粒子10aの外側の極薄い絶縁コート部分10a-2が削りとられて導電粒子本体10a-1が露出して導電性を発揮する。したがって、パンプ3と電極5に挟まれない部分では、絶縁コート部分10a-1が削りとられないため、導電性を発揮しない。よって、平面方向で電極5と電極3の間でのショートが発生しにくいということになる。また、通常、スタッズパンプを用いると、頭頂部の面積が小さいので導電粒子10aを電極5とパンプ3との間に挟み込むことが難しいので、導電粒子10aの量を多く入れることが必要であるが、そのようにすると、導電粒子同士が接触して電極3、5間にショートさせることがあるので、上記したように、絶縁コートされた絶縁性の導電粒子を使用するのが好ましい。また、リフロー特性などが良くなるのは、温度や湿度による膨潤により異方性導電膜形成用接着剤(又は異方性導電膜シート)がZ方向(異方性導電膜シートの厚み方向)に膨張した場合にも、導電粒子10aがそれ以上に膨張して接続を保つことができるためである。このため、導電粒子10aには、反発力のあるAu-Niコートのプラスチック粒子などを用いるのが好ましい。

【0074】次に、図1(C)の回路基板4の電極5上

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に、図1 (D) に示すように、ICチップ1の大きさより若干大きな寸法にカットされ、かつ、無機フィラー6 fが配合された異方性導電膜シート10を配置し、例えば80～120℃に熱せられた貼付けツール7により例えば5～10 kgf/cm²程度の圧力で異方性導電膜シート10を基板4に貼付ける。この後、異方性導電膜シート10の貼付けツール側に取り外し可能に配置されたのセパレータ10gを剥がすことにより基板4の準備工程が完了する。このセパレータ10gは、ツール7に無機フィラー6 fを配合した固体又は半固体の熱硬化性樹脂を含む異方性導電膜シート10が貼り付くのを防止するためのものである。ここで、図1 (G) に図1

(F) のG部分を部分的に拡大して示すように、異方性導電膜シート10は、導電粒子10aの平均直径より小さい平均直径の球状又は破碎シリカ、アルミナ等のセラミクスなどの無機系フィラー6 fを絶縁性樹脂6mに分散させて混合し、これをドクターブレード法などにより平坦化し溶剤成分を気化させ固体化したものが好ましいとともに、後工程のリフロー工程での高温に耐えうる程度の耐熱性（例えば、240℃に10秒間耐えうる程度の耐熱性）を有することが好ましい。上記絶縁性樹脂は、例えば、絶縁性熱硬化性樹脂（例えば、エポキシ樹脂、フェノール樹脂、ポリイミドなど）、又は絶縁性熱可塑性樹脂（例えば、ポニフェニレンサルファイト（PPS）、ポリカーボネイト、変性ポリフェニレンオキサイド（PPO）など）、又は、絶縁性熱硬化性樹脂に絶縁性熱可塑性樹脂を混合したものなどが使用できるが、ここでは、代表例として絶縁性熱硬化性樹脂として説明を続ける。この熱硬化性樹脂6mのガラス転移点は一般に120～200℃程度である。なお、熱可塑性樹脂のみを使用する場合には、最初は加熱して一旦軟化させたのち、加熱を停止して自然冷却させることにより硬化させる一方、絶縁性熱硬化性樹脂に熱可塑性樹脂を混合したものを使用する場合には、熱硬化性樹脂のほうが支配的に機能するため、熱硬化性樹脂のみと場合と同様に加熱することにより硬化する。

【0075】次に、図1 (E) 及び図1 (F) に示されるように、図20の電子部品搭載装置600において、部品保持部材601の先端の熱せられた接合ツール8により、上記工程でバンプ3が形成されたICチップ1をトレー602から吸着保持しつつ、該ICチップ1を、上記前工程で準備されかつステージ9上に載置された基板4のICチップ1の電極2に対応する電極5上に位置合わせて異方性導電膜シート10を介してICチップ1を基板4に押圧する。この位置合わせは、公知の位置認識動作を使用する。例えば、図21 (C) に示すように、基板4に形成された位置認識マーク605又はリード若しくはランドパターンを、電子部品搭載装置600の基板認識用カメラ604で認識して、図21 (D) に示すようにカメラ604で得られた画像606を基に、

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基板4のステージ9上での直交するXY方向のXY座標位置とXY座標の原点に対する回転位置とを認識して基板4の位置を認識する。一方、図21 (A) に示すように、接合ツール8に吸着保持されたICチップ1の位置認識用マーク608又は回路パターンをICチップ用位置認識用カメラ603で認識して、図21 (B) に示すようにカメラ603で得られた画像607を基に、ICチップ1の上記XY方向のXY座標位置とXY座標の原点に対する回転位置とを認識してICチップ1の位置を認識する。そして、上記基板4とICチップ1との位置認識結果を基に、接合ツール8又はステージ9を移動させて、ICチップ1の電極2が対応する基板4の電極5上に位置するように位置合わせしたのち、上記熱せられた接合ツール8によりICチップ1を基板4に押圧する。このとき、バンプ3は基板4の電極5上でバンプ3の頭部3aが図4 (B) から図4 (C) のごとく変形しながら押しつけられていく。このとき、第1実施形態で示した図2 (A) から図2 (B) と同様にこの実施形態においても、熱硬化性樹脂6m中の無機フィラー6fは、接合開始当初に熱硬化性樹脂6m中に入り込んできた尖っているバンプ3により、バンプ3の外側方向へ押し出される。また、第1実施形態で示した図2 (C) と同様にこの実施形態においても、この外側方向への押し出し作用によりバンプ3と基板電極5の間に無機フィラー6fが入り込まないことにより、接続抵抗値を低下させる効果を発揮する。このとき、もし、バンプ3と基板電極5の間に無機フィラー6fが多少入り込んだとしても、バンプ3と基板電極5とが直接接触していることにより、全く問題はない。このとき、印加する荷重は、バンプ3の外径により異なるが、頭部3aの折れ重なった部分が図4 (C) のように必ず変形するようとする。また、このとき、図6 (E) に示すように、異方性導電膜シート10中の導電粒子10aが樹脂ボール球に金属メッキを施されている場合には、導電粒子10aが変形することが必要である。また、異方性導電膜シート10中の導電粒子10aがニッケルなど金属粒子の場合には、図6 (D) に示すように、バンプ3や基板側の電極5にめり込むような荷重を加えることが必要である。この荷重は最低でも20 (gf/バンプ1ヶあたり) を必要とする。すなわち、図17には、80μmの外径のバンプの場合の抵抗値と荷重との関係のグラフより20 (gf/バンプ1ヶあたり) 未満では抵抗値100mΩ/バンプより大きくなつて抵抗値が大きくなりすぎて実用上問題があるため、20 (gf/バンプ1ヶあたり) 以上であることが好ましいことが示されている。また、図18には、80μm, 40μmのそれぞれの外径のバンプと最低荷重との関係に基づき信頼性の高い領域を示したグラフである。これより、40μm以上の外径のバンプでは最低荷重は25 (gf/バンプ1ヶあたり) 以上であることが好ましく、40μm未満の外径のバンプでは最

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低荷重は20 (g_f / バンプ1ヶあたり) 以上ぐらいが信頼性が高いことが推定される。なお、今後、リードの狭ピッチ化とともにバンプ外径が $40\mu m$ 未満と小さくなつた場合、バンプの投影面積に応じて、その2乗に比例して荷重が減少する傾向があることが推定される。よつて、ICチップ1を介してバンプ3側に印加する最低荷重は、最低で20 (g_f / バンプ1ヶあたり) を必要とするのが好ましい。上記ICチップ1を介してバンプ3側に印加する荷重の上限は、ICチップ1、バンプ3、回路基板4などが損傷しない程度とする。場合によつて、その最大荷重は100 (g_f / バンプ1ヶあたり) 若しくは150 (g_f / バンプ1ヶあたり) を越えることもある。このとき、導電粒子の平均直径より小さい平均直径の無機フィラー6fを使用していれば、熱硬化性樹脂6mの弾性率を増加させるとともに熱膨張係数を下げる効果を発揮することができる。

【0076】なお、図中、参照符号10sは、異方性導電膜シート10のうち接合ツール8の熱により溶融した溶融中の熱硬化性樹脂6mが溶融後に熱硬化された樹脂である。

【0077】なお、セラミックヒータ又はパルスヒータなどの内蔵ヒータ8aにより熱せられた接合ツール8により、上記前工程でバンプ3が電極2上に形成されたICチップ1を、上記前工程で準備された基板4に対してICチップ1の電極2が対応する基板4の電極5上に図1(E)に示すように位置するように位置合わせする位置合わせ工程と、位置合わせしたのち図1(F)に示すように押圧接合する工程とを、1つの位置合わせ兼押圧接合装置、例えば、図1(E)の位置合わせ兼押圧接合装置で行うようにしてもよい。しかしながら、別々の装置、例えば、多数の基板を連続生産する場合において位置合わせ作業と押圧接合作業とを同時的に行うことにより生産性を向上させるため、上記位置合わせ工程は図5(B)の位置合わせ装置で行い、上記押圧接合工程は図5(C)の接合装置で行うようにしてもよい。なお、図5(C)では、生産性を向上させるため、2つの接合装置8を示しており、1枚の回路基板4の2箇所を同時に押圧接合できるようにしている。

【0078】上記及び下記の各実施形態において、回路基板4としては、多層セラミック基板、ガラス布積層エポキシ基板(ガラエボ基板)、アラミド不織布基板、ガラス布積層ポリイミド樹脂基板、FPC(フレキシブル・プリンテッド・サーキット)又はアラミド不織布エポキシ基板(例えば、松下電器産業株式会社製の登録商標アリブ「ALIVH」として販売されている樹脂多層基板)などが用いられる。

【0079】これらの基板4は、熱履歴や、裁断、加工により反りやうねりを生じており、必ずしも完全な平面ではない。そこで、図5(A)及び図5(B)に示すように、例えば約 $10\mu m$ 以下に調整されるように平行度

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がそれぞれ管理された接合ツール8とステージ9とにより、接合ツール8側からステージ9側に向けて熱と荷重とをICチップ1を通じて回路基板4に局所的に印加することにより、その印加された部分の回路基板4の反りが矯正される。

【0080】また、ICチップ1は、アクティブ面の中心を凹として反っているが、これを接合時に1バンプあたり $20g_f$ 以上の強い荷重で加圧することで、基板4とICチップ1の両方の反りやうねりを矯正することができる。このICチップ1の反りは、ICチップ1を形成するとき、Siに薄膜を形成する際に生じる内部応力により発生するものである。バンプの変形量は $1.0 \sim 2.5\mu m$ 程度であり、この程度の基板が当初から持っている内層銅箔から表面に現れるうねりの影響にバンプ3の変形でそれぞれのバンプ3が順応することで許容できるようになる。

【0081】こうして、回路基板4の反りが矯正された状態で、例えば $140 \sim 230^\circ C$ の熱がICチップ1と回路基板4との間の異方性導電膜シート10に例えば数秒～20秒程度印加され、この異方性導電膜シート10が硬化される。このとき、最初は異方性導電膜シート10を構成する熱硬化性樹脂6mが流れていCチップ1のエッジまで封止する。また、樹脂であるため、加熱されたとき、当初は自然に軟化するため、このようにエッジまで流れるような流動性が生じる。熱硬化性樹脂6mの体積をICチップ1と回路基板4との間の空間の体積よりも大きくすることにより、この空間からはみ出すように流れ出て、封止効果を奏すことができる。この後、加熱された接合ツール8が上昇することにより、加熱源がなくなるためICチップ1と異方性導電膜シート10の温度は急激に低下して、異方性導電膜シート10は流動性を失い、図1(F)及び図4(C)に示されるように、ICチップ1は、異方性導電膜シート10を構成していく硬化工した樹脂10sにより、回路基板4上に固定される。また、回路基板4側をステージ9のヒータ9aなどにより加熱しておくと、接合ツール8の温度をより低くすることができる。

【0082】このようにすれば、異方性導電膜シート10に導電粒子10aの平均直径よりも小さい平均粒径の無機フィラーを配合した熱硬化性樹脂を用いることができ、さらに、異方性導電膜シート10に含まれる導電粒子10aとしてニッケル粉に金メッキを施したものを使うことにより、接続抵抗値を低下せしめることができて尚好適である。

【0083】上記第1実施形態によれば、熱硬化性樹脂6mに配合する無機フィラー6fとして導電粒子10aの平均直径より小さい平均粒径をもつ無機フィラー6fを配合することにより、導電粒子10aの働きを阻害することなくより信頼性を向上することができる。すなわち、バンプ3と基板4の電極5との間に導電粒子10a

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が挟まれる。このとき、同時に無機フィラー6 f が挟ま
れても導電粒子10 a の平均直径よりその平均粒径が小
さいため、導電性を阻害するところがなく、その上、熱硬
化性樹脂6 mの弾性率を増加し、熱膨張係数を低下して
ICチップ1と基板4の接合信頼性を向上する。

【0084】(第2実施形態) 次に、本発明の第2実施
形態にかかる回路基板への電子部品例えればICチップの
実装方法及び装置及び上記実装方法により上記ICチップ
が上記基板に実装された電子部品ユニット若しくはモ
ジュール例えれば半導体装置を説明する。

【0085】この第2実施形態においては、第1実施形
態において、熱硬化性樹脂を含む異方性導電膜シート1
0に配合する無機フィラー6 fの混合割合を上記絶縁性
熱硬化性樹脂例えれば絶縁性熱硬化性エポキシ樹脂6 mの
5~90wt%として、一層好適なものとしたものである。
5wt%未満では無機フィラー6 fを混合する意味
がない一方、90wt%を超えると、接着力が極度に低
下するとともに、シート化するのが困難になるため好ま
しくない。一例として、高い信頼性を維持させる観点か
ら、樹脂基板では20~40wt%、セラミック基板では
40~70wt%が好ましいとともに、ガラエボ基板
では20wt%程度でもシート封止剤の線膨張係数をか
なり低下させることができ、樹脂基板において効果があ
る。なお、体積%では、wt%のおよそ半分の割合、又
はエポキシ樹脂が1に対してシリカ約2の比重の割合と
する。通常では、熱硬化性樹脂6 mのシート化する際の
製造上の条件と基板4の弾性率、及び最終的には信頼性
試験結果により、この無機フィラー6 fの混合割合が決
定される。

【0086】上記したような混合割合の無機フィラー6
fを熱硬化性樹脂を含む異方性導電膜シート10に配合
することにより、異方性導電膜シート10の熱硬化性樹
脂6 mの弾性率を増加させることができ、熱膨張係数を
低下させてICチップ1と基板4の接合信頼性を向上さ
せることができる。また、基板4の材料に合わせて、熱
硬化性樹脂6 mの材料常数、すなわち弾性率、線膨張係数
を最適なものとするように、無機フィラー6 fの混合
割合を決定することができる。なお、無機フィラー6 f
の混合割合が挿入するにつれて、弾性率は大きくなる
が、線膨張係数は小さくなる傾向がある。

【0087】第1実施形態及び第2実施形態において
は、液体ではなく固体の異方性導電膜シート10を使用
するため取り扱いやすいとともに、液体成分が無いため
高分子で形成することができ、ガラス転移点の高いもの
を形成しやすいといった利点がある。

【0088】なお、図1(A)から図1(G)及び図2
(A)~図2(C)、後述する図6及び図7において
は、異方性導電層の一例としての熱硬化性樹脂を含む異
方性導電膜シート10又は異方性導電膜形成用熱硬化性
接着剤6 bを回路基板4側に形成することについて説明

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したが、これに限定されるものではなく、図14(A)
又は図14(B)に示すように、ICチップ1側に形成
したのち、基板4に接合するようにしてもよい。この場
合、特に、熱硬化性樹脂を含む異方性導電膜シート10
の場合には、異方性導電膜シート10の回路基板側に取
り外し可能に配置されたセパレータ6 aとともに、ステ
ージ201上のゴムなどの弾性体117に吸着ノズルな
どの保持部材200により保持されたICチップ1を押
し付けて、バンプ3の形状に沿って異方性導電膜シート
10がICチップ1に貼り付けられるようにしてよい。

【0089】(第3実施形態) 次に、本発明の第3実施
形態にかかる回路基板への電子部品例えればICチップの
実装方法及び装置及び上記実装方法により上記ICチップ
が上記基板に実装された電子部品ユニット若しくはモ
ジュール例えれば半導体装置を図6(A)~図6(C)及
び図7(A)~図7(F)を用いて説明する。

【0090】この第3実施形態では、第1実施形態にお
いて、熱硬化性樹脂を含む異方性導電膜シート10を基
板4に貼り付ける代わりに、図6(A)及び図7
(A), (D)に示すように、異方性導電層の一例として
の液体状の異方性導電膜形成用熱硬化性接着剤6 bを
回路基板4上に、ディスペンス502などによる塗布、
又は印刷、又は転写するようにしたのち、半固体状態、
いわゆるBステージ状態、まで固化し。その後、上記第
1又は第2実施形態と同様に、上記ICチップ1を上記
基板4に搭載する。

【0091】詳しくは、図6(A)に示すように、液体
状の異方性導電膜形成用熱硬化性接着剤6 bを回路基板
4上に、図7(A)に示すような空気圧で吐出量が制御
されかつ基板平面上で直交する2方向に移動可能なディ
スペンス502などによる塗布、又は印刷、又は転写する。
次いで、図6(B)のごとくヒータ78aを内蔵した
ツール78により、熱と圧力を印加して均一化しなが
ら、図6(C)のように半固体状態、いわゆるBステー
ジ状態、まで固化する。

【0092】又は、液体状の異方性導電膜形成用熱硬化
性接着剤6 bの粘性が低い場合には、図7(A)に示す
ように、ディスペンサ502で基板4上の所定位置に液
体の熱硬化性接着剤6 bを塗布したのち、熱硬化性接着
剤6 bの粘性が低いために自然に基板上で広がり、図7
(B)に示すような状態となる。その後、図7(C)に
示すように、コンベヤのような搬送装置505により上
記基板4を炉503内に入れて、炉503のヒータ50
4により上記塗布された絶縁性樹脂の液体状熱硬化性接
着剤6 bを硬化させることにより、半固体化、すなわ
ち、いわゆるBステージ状態まで固化する。

【0093】一方、液体状の異方性導電膜形成用熱硬化
性接着剤6 bの粘性が高い場合には、図7(D)に示す
ように、ディスペンサ502で基板4上の所定位置に液

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体の熱硬化性接着剤6 bを塗布したのち、熱硬化性接着剤6 bの粘性が高いために自然に基板上で広がらないため、図7 (E)、(F)に示すように、スキージ5 0 6で平らに延ばす。その後、図7 (C)に示すように、コンベヤのような搬送装置5 0 5により上記基板4を炉5 0 3内に入れて、炉5 0 3のヒータ5 0 4により上記塗布された絶縁性樹脂の液体状熱硬化性接着剤6 bを硬化させることにより、半固体化、すなわち、いわゆるBステージ状態、まで固化する。

【0094】このように異方性導電膜形成用熱硬化性接着剤6 bを半固体化するときには、熱硬化性接着剤6 b中の熱硬化性樹脂の特性により差はあるものの、該熱硬化性樹脂のガラス転移点の30～80%の温度である80～130°Cで押圧する。通常は、熱硬化性樹脂のガラス転移点の30%程度の温度で行う。このように熱硬化性樹脂のガラス転移点の30～80%とする理由は、図19の異方性導電膜シートの加熱温度と反応率とのグラフより、80～130°Cの範囲内ならば、まだ、後工程でさらに反応する範囲を充分に残すことができる。言い換えれば、80～130°Cの範囲内の温度ならば、時間にもよるが、絶縁性樹脂たとえばエポキシ樹脂の反応率が10～50%程度に抑制できるので、後工程のICチップ圧着時の接合に問題が生じない。すなわち、ICチップ圧着時に押圧するときに所定の押圧量を確保することができ、押し切れなくなるという問題を生じにくい。なお、反応を抑えて溶剤分のみを気化させることにより、半固体化することもある。

【0095】上記熱硬化性接着剤6 bを上記したように半固体化させたのち、基板4に複数のICチップ1を装着する場合には、基板4の複数のICチップ1を装着する複数の個所において上記熱硬化性接着剤6 bの上記半固体化工程を前段取り工程とし予め行っておき、このように前段取りされた基板4を供給して供給された基板4に複数のICチップ1を上記複数の個所に接合することでより生産性が高くなる。この後の工程では、熱硬化性接着剤6 bを使用する場合でも、基本的には上記した第1又は第2実施形態の異方性導電膜シート10を用いる工程と同一の工程を行う。上記半固定化工程を加えることで、液体の異方性導電膜形成用熱硬化性接着剤6 bを異方性導電膜シート10と同様に使用することができ、固体ゆえに取り扱いやすいとともに、液体成分が無いため高分子で形成することができ、ガラス転移点の高いものを形成しやすいといった利点がある。このように流動性のある異方性導電膜形成用熱硬化性接着剤6 bを使用する場合には、固体の異方性導電膜シート10を使用する場合と比較して、基板4の任意の位置に任意の大きさに塗布、印刷、又は転写することができる利点をも合わせて持つ。

【0096】(第4実施形態) 次に、本発明の第4実施形態にかかる回路基板への電子部品例えはICチップの

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実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置を図22を用いて説明する。第4実施形態が第1実施形態と異なる点は、ICチップ1を基板4に接合するとき、荷重に加えて超音波も印加して、バンプ3をレベリングせずに、必要に応じて20g f以下の荷重で押圧して、バンプ形成時の引き千切りにより生じた上記バンプ3の先端のネック(ヒゲ)部分の倒れによる隣接バンプ又は電極とのショートを防止するようにバンプ先端を整えたのち、ICチップ1と位置合わせてICチップ1を基板4に搭載して、金属バンプ3を基板側の電極表面の金属と超音波併用熱圧着することである。ICチップ1を基板4に接合する状態は、先の実施形態での図2及び図6などと同様である。上記超音波を印加して上記金バンプ3と上記基板4の上記電極とを金属接合するとき、上記ICチップ1の上記上面側から加熱しながら、又は、上記基板側から加熱しながら、又は、上記ICチップ1側と上記基板側の両方から加熱するようにしてよい。

【0097】この第4実施形態では、絶縁性熱硬化性樹脂6 mに無機フィラー6 fを配合した固体の異方性導電膜シート10又は液体の異方性導電膜形成用熱硬化性接着剤6 bを上記したように半固体化させたものを基板4に貼り付け、又は熱硬化性樹脂を含む異方性導電膜形成用熱硬化性接着剤6 bを基板4に塗布し半固体化させたのち、回路基板4の電極5と電子部品1の電極2にワイヤボンディングと同様に図3(A)～図3(F)のごとき動作により金線9 5の先端に電気スパークによりボール9 6を形成し、このボール9 6をキャピラリー9 3により基板電極5に超音波熱圧着して形成されたバンプ3を、レベリングせずに、ICチップ1と位置合わせてICチップ1を基板4に搭載する。ここで、上記「液体の異方性導電膜形成用熱硬化性接着剤6 bを上記したように半固体化させたもの」とは、第3実施形態で説明したような液体の異方性導電膜形成用熱硬化性接着剤6 bを半分固体化したものであり、Bステージ化したものとほぼ同じものである。このとき、図22に示す超音波印加装置6 2 0において、内蔵ヒータ6 2 2により予め加熱された接合ツール6 2 8により、該接合ツール6 2 8に吸着されたICチップ1の上面からエアシリンダ6 2 5による荷重と、ピエゾ素子のような超音波発生素子6 2 3により発生させられて超音波ホーン6 2 4を介して印加される超音波とを作用させて金バンプ3のネック部分の倒れを防止するように先端を整えつつ金バンプ3と基板側の金メッキとを金属接合する。次に、ICチップ1の上面又は、及び基板側から加熱しながら、上記ICチップ1を上記回路基板4に1バンプあたり20 g f以上の加圧力により押圧し、上記基板4の反りの矯正とバンプ3を押しつぶしながら、上記ICチップ1と上記回路基板4の間に介在する上記異方性導電膜シート10又

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は熱硬化性接着剤6 bを上記熱により硬化して、上記ICチップ1と上記回路基板4を接合して両電極2, 5を電気的に接続する。なお、超音波印加装置6 2 0による上記金属接合時に、上記ICチップ1の上記上面側から、又は、上記基板側から、又は、上記ICチップ1側と上記基板側の両方から加熱するようにしてもよい。すなわち、具体的には、内蔵ヒータ6 2 2により上記ICチップ1の上記上面側から加熱したり、又は、上記基板側から回路基板4側をステージ9のヒータ9 aにより加熱したり、又は、内蔵ヒータ6 2 2とステージ9のヒータ9 aとにより上記ICチップ1側と上記基板側の両方から加熱するようにしてもよい。

【0098】なお、1バンプあたり20 g f以上の加圧力を必要とする理由は、このように超音波を用いた接合でも摩擦熱が生じにくくなるので、接合できなくなるためである。金と金とを接合するような場合においても、ある一定加重でバンプを押しつけて、そこに超音波を印加することにより摩擦熱が生じて金属同士が接合される。したがって、この場合にもバンプを押圧する程度の一定荷重すなわち1バンプあたり20 g f以上の加圧力が必要となる。加圧力の一例としては、1バンプあたり50 g f以上とする。

【0099】上記第4実施形態によれば、金属バンプ3と基板4の金属メッキが金属拡散接合されるので、よりバンプ部分での強度を持たせたいような場合や、接続抵抗値をさらに低くしたいような場合に好適である。

【0100】(第5実施形態) 次に、本発明の第5実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置を図8(A)～図8(C)及び図9(A)～図9(C)を用いて説明する。第5実施形態は、第1実施形態とは封止工程を省略することができる点が異なる。

【0101】上記したようにICチップ1上の電極2に突起電極(バンプ)3を形成しておき、回路基板4には、図8(B), 図8(C), 図9(A)及び図23に示すように、ICチップ1の複数の電極2の内端縁を結んだ大略矩形の外形寸法O Lより小さい形状寸法の矩形のシート状の異方性導電膜シート10又は熱硬化性接着剤6 bを回路基板4の電極5を結んだ中心部分に貼り付け又は塗布しておく。このとき、シート状の異方性導電膜シート10又は熱硬化性接着剤6 bの厚みは、その体積がICチップ1と基板4との隙間より大きくなるようになる。また、図23の貼り付け装置640により、巻き戻しロール644から巻き戻されて巻き付けロール643に巻き取られる矩形のシート状の異方性導電膜シート656を、その切り目657が予め入れられた部分で、上下のカッター641により、ICチップ1の複数の電極2の内端縁を結んだ大略矩形の外形寸法O Lより

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小さい形状寸法に切断する。切断された矩形のシート状の異方性導電膜シート10は、内蔵ヒータ646で予め加熱された貼り付けヘッド642で吸着保持されて、上記回路基板4の電極5を結んだ中心部分に貼り付けされる。次に、バンプ3と回路基板4の電極5を位置合わせし、図8(A)及び図9(B)に示すように、ヒータ8aにより加熱された接合ツール8によりICチップ1を回路基板4に加圧押圧して、基板4の反りの矯正を同時に進行ながら、ICチップ1と回路基板4の間に介在する異方性導電膜シート10又は熱硬化性接着剤6 bを硬化する。このとき、異方性導電膜シート10又は熱硬化性接着剤6 bは、接合ツール8からICチップ1を介して加えられた熱により上記したように軟化し、図9(C)のごとく貼り付けられた又は塗布された位置より加圧されて外側へ向かって流れ出る。この流れ出た異方性導電膜シート10又は熱硬化性接着剤6 bが封止材料(アンダーフィル)となり、バンプ3と電極5との接合の信頼性を著しく向上する。また、ある一定時間がたつと、上記異方性導電膜シート10又は熱硬化性接着剤6 bでは徐々に硬化が進行し、最終的には硬化した樹脂6sによりICチップ1と回路基板4を接合することになる。ICチップ1を押圧している接合ツール8を上昇することで、ICチップ1と回路基板4の電極5の接合が完了する。厳密に言えば、熱硬化の場合には、熱硬化性樹脂の反応は加熱している間に進み、接合ツール8が上昇するとともに流動性はほとんど無くなる。上記したような方法によると、接合前では異方性導電膜シート10又は熱硬化性接着剤6 bが電極5を覆っていないので、接合する際にバンプ3が電極5に直接接触し、電極5の下に異方性導電膜シート10又は熱硬化性接着剤6 bが入り込まず、バンプ3と電極5との間での接続抵抗値を低くすることができる。また、回路基板側を加熱しておくと、接合ヘッド8の温度をより低くすることができる。この方法を上記第3実施形態に適用すると金バンプと回路基板の金電極(例えは、銅やタンガステンにニッケル、金メッキしたもの)との接合がより容易に行える。

【0102】(第6実施形態) 次に、第6実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置を図10～図11を用いて説明する。第6実施形態においては、第1実施形態と異なる点は、バンプ103を回路基板4の電極5にズレて実装された場合においても、信頼性の高い接合を達成することもできる点である。

【0103】第6実施形態においては、図10(A)に示すように、バンプ3をICチップ1上に形成する際にワイヤボンディングと同様に金線95を電気スパークにより金ボール96を形成する。次に、電気スパークする

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ときの時間でボールの大きさを調整しつつ、95aで示す直径Φd-Bumpのボール96aを形成し、このように形成された直径Φd-Bumpのボール96aを、電気スパークを発生させるための時間又は電圧のパラメータを制御して、チャムファ一角θcが100°以下のキャピラリー193の93aで示すチャムファー直径ΦDが金ボール直径d-Bumpの1/2から3/4となるようにボール96aを形成し、図10(C)に示すようにキャピラリー93の金ボールと接する部分に平らな部位93bを設けて図10(D)に示すようなバンプ3を形成するのではなく、図10(A)に示すようにキャピラリー193の金ボール96aと接する部分に平らな部位を設けない先端部位193aを有する先端形状としたキャピラリー193で、ICチップ1の電極2に、超音波熱圧着により、図10(B)に示すようなバンプ103を形成する。上記先端形状のキャピラリー193を用いることで、図10(B)のbのような先端が大略円錐状のバンプ103をICチップ1の電極2に形成することができる。上記方法で形成した先端が大略円錐状のバンプ103を回路基板4の電極5に図11(C)のごとくズレて実装された場合においても、バンプ103がその先端が大略円錐形であるため、バンプ103の外径の半分までのズレである場合は、バンプ103の一部が必ず基板4の電極5と接触することができる。

【0104】これに対して、図11(D)に示すようなバンプ3では、バンプ3を回路基板4の電極5に図11(C)のごとく寸法Zだけズレて実装された場合には、図11(E)に示すように、幅寸法dのいわゆる台座3gの一部が電極5に接触するが、部分的にしか接触せず、接触状態が不安定な接合となる。このような不安定な接合状態のままでは、このような基板4を冷熱衝撃試験やリフローにかけた場合には、上記不安定な接合状態の接合がオープンすなわち接合不良となってしまう可能性があった。これに対して、上記第6実施形態では、図11(C)のごとく先端が大略円錐状のバンプ103が回路基板4の電極5に対して寸法Zだけズレて実装された場合においても、バンプ103が円錐形であるため、バンプ103の外径の半分までのズレである場合は、バンプ103の一部が必ず基板4の電極5と接触することができ、冷熱衝撃試験やリフローにかけた場合でも接合不良となることが防止できる。

【0105】(第7実施形態) 次に、第7実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置を図12～図13を用いて説明する。この第7実施形態では、第1実施形態において、回路基板4へのICチップ1の接合したのちの熱硬化性樹脂の硬化時にICチップ1と回路基板4の応力を緩和することができるようとしたものである。

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【0106】第7実施形態においては、絶縁性熱硬化性樹脂6mに無機フィラー6fを配合した固体又は半固体の異方性導電膜シート10又は熱硬化性接着剤6bを介在させながら、ICチップ1の電極2に上記ワイヤボンディングにより形成されたバンプ3を、レベリングせずに、回路基板4の電極5と位置合わせする。例えば230°C程度の一定温度に加熱されたツール8によりICチップ1をその裏面から加熱しながら、上記ICチップ1を上記回路基板4に1バンプあたりセラミック基板の場合には圧力P1=80gf以上の加圧により押圧し、上記基板4の反りの矯正を行いながら、上記ICチップ1と上記回路基板4の間に介在する上記異方性導電膜シート10又は熱硬化性接着剤6bを上記熱により硬化する。次に、一定時間t1後、すなわち、全体時間を例えれば20秒とすれば、材料の反応率により変わるが、その1/4とか1/2の5秒～10秒後、言い換えれば、材料の反応率が90%に達する前に、上記圧力P1より低い圧力P2まで下げて熱硬化性接着剤6bの硬化時の応力を緩和し、上記ICチップ1と上記回路基板4を接合して両電極2, 5を電気的に接続する。好適には、バンプが変形していくためには最低限20gf程度は必要であるため、すなわち、バンプの変形及び順応に必要な圧力を得るとともに、余分な樹脂をICチップ1と基板4との間から押し出すため、上記圧力P1は20gf/バンプ以上である一方、バンプの変形等の前に樹脂内部に偏在した硬化歪み除去するため、圧力P2は20gf/バンプ未満とすることにより、より信頼性が向上する。その理由は詳しくは以下のとおりである。すなわち、図12(C)に示すように、異方性導電膜シート10又は熱硬化性接着剤6b中の熱硬化性樹脂の応力分布は圧着時にICチップ1と基板4側とで大きくなっている。このままでは、信頼性試験や通常の長期使用で繰り返し疲労が与えられると、ICチップ1又は基板4側で異方性導電膜シート10又は熱硬化性接着剤6b中の熱硬化性樹脂が応力に耐えきれずに剥離することがある。このような状態になると、ICチップ1と回路基板4の接着力が十分でなくなり、接合部がオープンすることになる。そこで、図13のように、より高い圧力P1とより低い圧力P2との2段階の圧力プロファイルを用いることにより、熱硬化性接着剤6bの硬化時に上記圧力P1より低い圧力P2まで下げることができて、図12(D)のごとく、圧力P2のときに樹脂内部に偏在した硬化歪み除去してICチップ1と回路基板4の応力を緩和する(言い換えれば、応力の集中度合いを減らす)ことができ、その後、上記圧力P1まで上げることにより、バンプの変形及び順応に必要な圧力を得るとともに、余分な樹脂をICチップ1と基板4との間から押し出すことができ、信頼性が向上する。

【0107】なお、上記「ICチップ1と回路基板4の接着力」とは、ICチップ1と基板4をひっつける力の

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ことを意味する。これは、接着剤による接着力と、接着剤を硬化したときの硬化収縮力と、Z方向の収縮力（例えれば180℃に熱せられている接着剤が常温に戻るときに収縮するときの収縮力）のこれら3つの力によって、IC1と基板4とは接合されている。

【0108】（第8実施形態）次に、第8実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置を図12～図13を用いて説明する。この第8実施形態では、上記各実施形態において、上記絶縁性樹脂6mに配合する上記無機フィラー6fの平均粒径が3μm以上であるようにしたものである。ただし、上記無機フィラー6fの最大平均粒径は、ICチップ1と基板4との接合後の隙間寸法を超えない大きさとする。

【0109】もし、無機フィラー6fを絶縁性樹脂6mに配合するときに、平均粒径が3μm未満の細かな粒子を無機フィラー6fとして用いると、それらの粒子の表面積自体が全体として大きくなり、平均粒径が3μm未満の細かな粒子である無機フィラー6fの周りに吸湿することがあり、ICチップ1と基板4との接合において好ましくない。

【0110】従って、同じ重量の無機フィラー6fを配合する場合には、平均粒径が3μm以上の大きな無機フィラー6fを用いることで、無機フィラー6fの周りにおける吸湿量を減らしめることができ、耐湿性を向上させることが可能となる。また、一般に、平均粒径（言い換えれば平均粒度）の大きな無機フィラーの方が安価であるため、コスト的にも好ましい。

【0111】なお、図24(A)に示すように、ICチップ1と基板4との接合において従来のACF(Anisotropic Conductive Film:異方性導電膜)598を使用する工法では、ACF598中の導電粒子599をバンプ3と基板電極5との間に必ず挟むと同時に直径3～5μmの導電粒子が直径1～3μmまで押しつぶされて導電性を発揮させる必要がある。しかしながら、本発明の上記各実施形態では、導電粒子10aがあつても必ずしもバンプ3と基板電極5との間に挟む必要は無く、図24(B)に示すようにバンプ3を基板電極5で押しつぶしながら圧着するので、この圧着のときにバンプ3と基板電極4との間の異方性導電層10とともに無機フィラー6fもバンプ3と基板電極4と間から抜け出ることになり、基板電極4とバンプ3の間に不要な無機フィラー6fが挟まることにより導電性を阻害することがほとんど無いという特徴に基づき、3μm以上の大きな平均粒径の無機フィラー6fを使用することができる。すなわち、本実施形態では、万が一、導電粒子10aがバンプ3と基板電極5との間に挟まれず、直径3～5μmの導電粒子10aが直径1～

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3μmまで押しつぶされて導電性を発揮することがなくとも、バンプ3を基板電極5で押しつぶしながら圧着してバンプ3が基板電極5に電気的に直接接触して電気的導電性を得ているため、何ら問題はなく、無機フィラーによる影響を受けずに信頼性を向上することができる。すなわち、上記導電粒子10aは、バンプ3と基板電極5との直接接合において、導電粒子10aがバンプ3と基板電極5との間に挟まれた場合には、基板側の電極5とICチップ側のバンプ3との間での接続抵抗値を低下せしめることができるといった、付加的効果を奏するものである。

【0112】（第9実施形態）次に、本発明の第9実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置を図25、26を用いて説明する。図25、26は、それぞれ、上記第9実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置により製造された接合状態の模式断面図及びそのときに使用される異方性導電膜シート10の部分拡大模式断面図である。この第9実施形態では、上記各実施形態において、上記異方性導電層10の上記絶縁性樹脂6mに配合する上記無機フィラー6fは、複数の異なる平均粒径を持つ無機フィラー6f-1、6f-2とするものである。具体例としては、0.5μmの平均粒径を持つ無機フィラーより、2～4μmの平均粒径を持つ無機フィラーとする。

【0113】上記第9実施形態によれば、複数の異なる平均粒径を持つ無機フィラー6f-1、6f-2を絶縁性樹脂6mに混合することにより、絶縁性樹脂6mに混合する無機フィラー6fの量を増加させることができて、無機フィラーの周りにおける吸湿量を減らしめることができ、耐湿性を向上させることができるとともに、フィルム化（固体化）することが容易になる。すなわち、重量%で考えた場合、一種類の無機フィラーよりも、粒径の異なる無機フィラーを混在して入れた方が、単位体積あたりの無機フィラーの量を増やすことが可能である。これによって、封止シートとしての異方性導電膜シート10又は異方性導電膜形成用接着剤6bへの無機フィラー6fの配合量を増加し、異方性導電膜シート10又は異方性導電膜形成用接着剤6bの線膨張係数を低下させることができ、より長寿命化させることができて、信頼性を向上させることができる。

【0114】（第10実施形態）次に、本発明の第10実施形態にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置においては、上記第9実施形態における効果をより確実なものとするため、さらに、上記複数の異なる平均粒径を持つ無機フィラー6f

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-1, 6 f -2 のうちの一方の無機フィラー 6 f -1 の平均粒径は、他方の無機フィラー 6 f -2 の平均粒径の2倍以上異なっているものである。具体例としては、0.5 μm の平均粒径を持つ無機フィラーと、2~4 μm の平均粒径を持つ無機フィラーとする。

【0115】このようにすることにより、上記第9実施形態での効果をより一層高めることができる。すなわち、一方の無機フィラー 6 f -1 の平均粒径は、他方の無機フィラー 6 f -2 の平均粒径の2倍以上異なっている複数の異なる平均粒径を持つ無機フィラー 6 f -1, 6 f -2 を絶縁性樹脂 6 m に混合することにより、絶縁性樹脂 6 m に混合する無機フィラー 6 f の量をより確実に増加させることができて、フィルム化(固体化)することができより容易になり、異方性導電膜シート 10 又は異方性導電膜形成用接着剤 6 b への無機フィラー 6 f の配合量を増加し、異方性導電膜シート 10 又は異方性導電膜形成用接着剤 6 b の線膨張係数をより低下させることができ、より長寿命化させてることができ、信頼性をより向上させることができる。

【0116】(第11実施形態) 次に、本発明の第11実施形態にかかる回路基板への電子部品例ええばICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えれば半導体装置においては、上記第9実施形態における効果をより確実なものとするため、さらに、上記絶縁性樹脂 6 m に配合する上記無機フィラー 6 f は、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー 6 f -1, 6 f -2 であって、上記少なくとも2種類の無機フィラーのうちの一方の無機フィラー 6 f -1 は 3 μm を超える平均粒径を持ち、上記少なくとも2種類の無機フィラーのうちの他方の無機フィラー 6 f -2 は 3 μm 以下の平均粒径を持つことが好ましい。具体例としては、0.5 μm の平均粒径を持つ無機フィラーと、2~4 μm の平均粒径を持つ無機フィラーとする。

【0117】(第12実施形態) 次に、本発明の第12実施形態にかかる回路基板への電子部品例ええばICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えれば半導体装置においては、上記各実施形態において、さらに、上記絶縁性樹脂 6 m に配合する上記無機フィラー 6 f は、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー 6 f -1, 6 f -2 であって、上記少なくとも2種類の無機フィラーのうちの平均粒径の大きい一方の無機フィラー 6 f -1 は上記絶縁性樹脂 6 m と同一材料からなることにより、応力緩和作用を奏すようにすることもできる。具体例としては、0.5 μm の平均粒径を持つ無機フィラーと、2~4 μm の平均粒径を持つ無機フィラーとする。

【0118】この第12実施形態によれば、第9実施形

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態での作用効果に加えて、平均粒径の大きい一方の無機フィラー 6 f -1 は上記絶縁性樹脂 6 m と同一材料からなることにより、上記絶縁性樹脂 6 m に応力が作用したとき、平均粒径の大きい一方の無機フィラー 6 f -1 が上記絶縁性樹脂 6 m と一体化することにより、応力緩和作用を奏すことができる。

【0119】(第13実施形態) 次に、本発明の第13実施形態にかかる回路基板への電子部品例ええばICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えれば半導体装置においては、上記各実施形態において、さらに、上記絶縁性樹脂 6 m に配合する上記無機フィラー 6 f は、複数の異なる平均粒径を持つ少なくとも2種類の無機フィラー 6 f -1, 6 f -2 であって、上記少なくとも2種類の無機フィラーのうちの平均粒径の大きい一方の無機フィラー 6 f -1 は上記絶縁性樹脂 6 m であるエポキシ樹脂よりも柔らかく、上記一方の無機フィラー 6 f -1 が圧縮されることにより、応力緩和作用を奏すようにすることもできる。

【0120】この第13実施形態によれば、第9実施形態での作用効果に加えて、平均粒径の大きい一方の無機フィラー 6 f -1 は上記絶縁性樹脂 6 m と同一材料からなることにより、上記絶縁性樹脂 6 m に応力が作用したとき、平均粒径の大きい一方の無機フィラー 6 f -1 が上記絶縁性樹脂 6 m であるエポキシ樹脂よりも柔らかいため、上記応力により、上記一方の無機フィラー 6 f -1 が図27に示すように圧縮されてその周囲で圧縮に対する反力を有する引張力が分散されることにより、応力緩和作用を奏すことができる。

【0121】(第14実施形態) 次に、本発明の第14実施形態にかかる回路基板への電子部品例ええばICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えれば半導体装置においては、上記各実施形態において、さらに、図28(A), (B), 図29(A), (B), 図30及び図31に示されるように、上記異方性導電層 10 は、上記ICチップ 1 又は上記基板 4 に接触する部分 700 又は層 6x が、他の部分 701 又は層 6y よりも上記無機フィラー量が少ないか、もしくは上記無機フィラー 6 f を配合しないようにすることができる。この場合、図28(A), (B) に示すように、上記ICチップ 1 又は上記基板 4 に接触する部分 700 と、他の部分 701 を明確に区別することなく、徐々に無機フィラー量が変わるようにしてよいし、図29(A), (B) 及び図30, 図31に示すように明確に区別するようにしてよい。すなわち、図29(A), (B) 及び図30, 図31において、上記異方性導電層 10 は、上記ICチップ 1 又は上記基板 4 に接触する部分に位置されかつ上記絶縁性樹脂 6 m と同一の絶縁性樹脂に上記無機フィラー 6 f を配合した第1樹

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脂層 6 x と、上記第1樹脂層 6 x に接触し、かつ、上記第1樹脂層 6 x よりも上記無機フィラー量が少ないか、もしくは上記無機フィラー 6 f を配合しない上記絶縁性樹脂で構成される第2樹脂層 6 y とを備えて多層構造にすることもできる。

【0122】このようにすれば、以下のような効果を奏すことができる。すなわち、もし、上記無機フィラー 6 f を異方性導電層全体に同じ重量パーセント($w\text{ t}\%$)を入れると、ICチップ側又は基板側又はその両方の対向面の近傍に無機フィラー 6 f が多くなることがあり、ICチップ1と基板4との中間部分では逆に少なくなる。この結果、ICチップ側又は基板側又はその両方の対向面の近傍に無機フィラー 6 f が多いため、異方性導電層 1 o とICチップ1又は基板4又はその両方との間での接着力が低下することがある。上記第14実施形態によれば、上記ICチップ1又は上記基板4のいずれか一方に接触する部分 7 0 0 又は層 6 x が、他の部分 7 0 1 又は層 6 y よりも上記無機フィラー量が少ないか、もしくは上記無機フィラー 6 f を配合しないようにすることにより、無機フィラー量が多いために接着力が低下することを防止できる。

【0123】以下に、この第14実施形態の種々の変形例について説明する。

【0124】まず、第1の変形例として、図28

(C)、図29(C)及び図32(A)に示されるように、上記異方性導電層 1 o は、上記ICチップ1及び上記基板4の両方にそれぞれ接触する部分 7 0 0 が、他の部分 7 0 1 よりも上記無機フィラー量が少ないか、もしくは上記無機フィラー 6 f を配合しないようにすることもできる。この場合も、図28(C)に示すように、上記ICチップ1及び上記基板4の両方に接触する部分 7 0 0 と、他の部分 7 0 1 とを明確に区別することなく、徐々に無機フィラー量が変わるようにしてもよいし、図29(C)及び図32(A)において、上記異方性導電層 1 o は、上記第1樹脂層 6 x の上記第2樹脂層 6 y とは反対側に、上記第1樹脂層 6 x よりも上記無機フィラー量が少ないか、もしくは上記無機フィラー 6 f を配合しない上記絶縁性樹脂で構成される第3樹脂層 6 z をさらに備えて多層構造とし、上記第1樹脂層 6 x と上記第3樹脂層 6 z は、それぞれ、上記ICチップ1と上記基板4とに接触するようにすることもできる。

【0125】さらに、別の変形例として、上記ICチップ1又は上記基板4又はその両方にそれぞれ接触する部分 7 0 0 は、その上記無機フィラー量が 20 w t\% 未満か、もしくは上記無機フィラー 6 f を配合しないようする一方、上記他の部分 7 0 1 はその上記無機フィラー量が 20 w t\% 以上であるようにすることもできる。この場合、図28(A)、(B)、(C)に示すように上

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記ICチップ1又は上記基板4又は両方に接触する部分 7 0 0 と、他の部分 7 0 1 とを明確に区別することなく、徐々に無機フィラー量が変わるようにしてもよいし、図29(A)、(B)、図29(C)、図30、図31、及び図32(A)に示すように明確に区別するようにもよい。すなわち、上記第1樹脂層 6 x 又は第1樹脂層 6 x 及び上記第3樹脂層 6 z は、その上記無機フィラー量が 20 w t\% 未満か、もしくは上記無機フィラー 6 f を配合しないようする一方、上記第2樹脂層 6 y はその上記無機フィラー量が 20 w t\% 以上であるようにすることもできる。

【0126】具体例としては、上記第2樹脂層 6 y は、絶縁性樹脂 6 m として熱硬化性エポキシ樹脂としたとき、セラミック基板の場合には 50 w t\% であり、ガラスエポ基板の場合は 20 w t\% とする。また、一例として、第1樹脂層 6 x 又は第3樹脂層 6 z 又はその両方の厚さは $15\mu\text{m}$ 、第2樹脂層 6 y の厚さは $40\sim60\mu\text{m}$ とする。また、上記異方性導電層 1 o の厚さは、ICチップ1と基板4との接合後の隙間寸法よりも大きな寸法として、ICチップ1と基板4との接合時にICチップ1と基板4との間に完全に満たされるようにして接合をより確実なものとする。

【0127】また、別の変形例として、図28(C)、図29(C)及び図32(A)に示す変形例と無機フィラーの配合量を逆にするようにしてもよい。すなわち、図28(D)に示されるように、上記異方性導電層 1 o は、上記ICチップ1及び上記基板4の両方にそれぞれ接触する部分 7 0 3 の中間部分 7 0 2 が、上記ICチップ1及び上記基板4の両方にそれぞれ接触する部分 7 0 3 よりも上記無機フィラー量が少ないか、もしくは上記無機フィラー 6 f を配合しないようにすることもできる。この場合も、上記ICチップ1又は上記基板4又は両方に接触する部分 7 0 3 と、中間部分 7 0 2 とを明確に区別することなく、徐々に無機フィラー量が変わるようにしてもよいし、図29(D)及び図32(B)に示されるように、明確に区別するようにしてもよい。すなわち、図29(D)及び図32(B)に示されるように、上記異方性導電層 1 o は、上記ICチップ1及び上記基板4に接触する部分に位置されかつ上記無機フィラー 6 f を配合した絶縁性樹脂 6 m で構成される第4樹脂層 6 v と、上記ICチップ1と上記基板4との中間部分に位置されかつ上記第4樹脂層 6 v よりも上記無機フィラー量が少ないか又は含まれていない絶縁性樹脂 6 m で構成される第5樹脂層 6 w とを備えるようにすることもできる。

【0128】このようにすれば、上記ICチップ1と上記基板4との上記中間部分 7 0 2 又は上記第5樹脂層 6 w では、上記ICチップ1と上記基板4とにそれぞれ接触する部分 7 0 3 又は上記第4樹脂層 6 v よりも上記無機フィラー量が少ないか又は含まれていないため、弹性

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率が低くなり、応力緩和効果を奏することができる。また、上記ICチップ1と上記基板4とにそれぞれ接触する部分703又は上記第4樹脂層6vの絶縁性樹脂としてICチップ1と基板4に対する密着力の高いものを選択して使用すれば、上記ICチップ1に接触する部分703又はICチップ1の近傍部分の上記第4樹脂層6vでは、ICチップ1の線膨張係数にできるだけ近くなるように無機フィラー6fの配合量又は材料を選択する一方、上記基板4に接触する部分703又は基板4の近傍部分の上記第4樹脂層6vでは、基板4の線膨張係数にできるだけ近くなるように無機フィラー6fの配合量又は材料を選択することができる。この結果、上記ICチップ1に接触する部分703又はICチップ1の近傍部分の上記第4樹脂層6vとICチップ1との線膨張係数が接近するため、両者の間での剥離が生じにくくなるとともに、上記基板4に接触する部分703又は基板4の近傍部分の上記第4樹脂層6vと基板4との線膨張係数が接近するため、両者の間での剥離が生じにくくなる。

【0129】さらに、図33(A), (B)に実線で示すように、上記異方性導電層10は、上記ICチップ1又は上記基板4のいずれか一方に接触する部分P1から他の部分P2に向かって、上記無機フィラー量が徐々に又は段階的に少なくなるようにすることもできる。

【0130】また、図33(C), (D)に実線で示すように、上記異方性導電層10は、上記ICチップ1及び上記基板4にそれぞれ接触する部分P3, P4から他の部分すなわちICチップ1と上記基板4との中間部分P5に向かって、上記無機フィラー量が徐々に又は段階的に多くなるようにすることもできる。

【0131】また、図33(E)に実線で示すように、上記異方性導電層10は、上記ICチップ1及び上記基板4にそれぞれ接触する部分(図28(D)の変形例における接触部分703に相当する部分)から、上記ICチップ1及び上記基板4との中間部分(図28(D)の変形例における中間部分702に相当する部分)に向かって、上記無機フィラー量が徐々に少なくなるようにすることもできる。

【0132】また、図33(F)に実線で示すように、上記異方性導電層10は、上記ICチップ1の近傍部分、次いで、上記基板4の近傍部分、次いで、上記ICチップ1の近傍部分と上記基板4の近傍部分との中間部分の順に上記無機フィラー量が少ないようになることもできる。なお、図33(F)では、上記順に徐々に上記無機フィラー量が変化するように例示しているが、これに限られるものではなく、段階的に変化するようにしてもよい。

【0133】上記図33(E), (F)の変形例のようにすれば、上記ICチップ1と上記基板4との中間部分では、上記ICチップ1及び上記基板4にそれぞれ接触

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する部分よりも上記無機フィラー量が少ないか又は含まれていないため、弾性率が低くなり、応力緩和効果を奏することができる。また、上記ICチップ1及び上記基板4にそれぞれ接触する部分の絶縁性樹脂としてICチップ1と基板4に対する密着力の高いものを選択して使用すれば、ICチップ1に接触する部分では、ICチップ1の線膨張係数にできるだけ近くなるように無機フィラー6fの配合量又は材料を選択する一方、基板4に接触する部分では、基板4の線膨張係数にできるだけ近くなるように無機フィラー6fの配合量又は材料を選択することができる。この観点で無機フィラー6fの配合量を決定すると、通常は、図33(F)に実線で示すように、上記ICチップ1の近傍部分、次いで、上記基板4の近傍部分、次いで、上記ICチップ1の近傍部分と上記基板4の近傍部分との中間部分の順に上記無機フィラー量が少ないようなる。このような構成とすることにより、ICチップ1に接触する部分とICチップ1との線膨張係数が接近するため、両者の間での剥離が生じにくくなるとともに、基板4に接触する部分と基板4との線膨張係数が接近するため、両者の間での剥離が生じにくくなる。

【0134】図33(A)～(F)のいずれの場合でも、実用上、上記無機フィラー量は5～90wt%の範囲内とすることが好ましい。5wt%未満では無機フィラー6fを混合する意味がない一方、90wt%を超えると、接着力が極度に低下するとともに、シート化するのが困難になるため好ましくないためである。

【0135】なお、上記のような複数の樹脂層6x, 6y又は6x, 6y, 6zで構成される多層構造の膜を異方性導電層として用いてICチップ1を基板4に熱圧着した場合には、接合時の熱により絶縁性樹脂6mが軟化、溶融して上記樹脂層が混じり合うので、最終的には、各樹脂層の明確な境界が無くなり、図33のように傾斜した無機フィラーフィルムとなる。

【0136】さらに、上記第14実施形態又は各変形例において、無機フィラー6fの入った部分又は層を有する異方性導電層、又は、無機フィラーフィルムが傾斜した異方性導電層において、上記部分又は樹脂層に応じて、異なる絶縁性樹脂を用いることも可能である。例えば、ICチップ1に接触する部分又は樹脂層では、ICチップ表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を用いる一方、基板4に接触する部分又は樹脂層では、基板表面の材料に対して密着性を向上させる絶縁性樹脂を用いることも可能となる。

【0137】上記第14実施形態及びそれらの上記種々の変形例によれば、ICチップ1又は上記基板4と異方性導電層10との接合界面では無機フィラー6fが存在しないかその量が少なく、絶縁性樹脂本来の接着性が発揮されて、上記接合界面で接着性の高い絶縁性樹脂が多くなり、ICチップ1又は上記基板4と絶縁性樹脂6m

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との密着強度を向上させることができて、ICチップ1又は上記基板4との接着性が向上する。これにより、各種信頼性試験での寿命が向上するとともに、曲げに対しての剥離強度が向上する。

【0138】もし、接着そのものには寄与しないが線膨張係数を下げる効果を持つ無機フィラー6fが絶縁性樹脂6m中に均一に分散されていると、基板4又はICチップ表面に無機フィラー6fが接触し、接着に寄与する接着剤の量が減少することになり、接着性の低下を招く。この結果、もしICチップ1または基板4と接着剤の間で剥離が生じると、そこから水分が侵入し、ICチップ1の電極の腐食などの原因となる。また、剥離部分から剥がれが進行すると、ICチップ1と基板4の接合そのものが不良となり、電気的に接続不良となる。

【0139】これに対して、上記第14実施形態及びそれらの上記種々の変形例によれば、上記したように、無機フィラー6fによる線膨張係数を下げる効果を持たせたまま接着力を向上させることができる。これによって、ICチップ1及び基板4との密着強度が向上し、信頼性が向上する。

【0140】さらに、無機フィラー6fの少ない部分700又は樹脂層6xをICチップ側に配置した場合、又は、ICチップ側において無機フィラーフ分布を小さくした場合には、当該部分700又は樹脂層6xは、ICチップ表面の窒化シリコンや酸化珪素からなるバッショーション膜に対して接着力を向上させることができるとなる。また、これらICチップ表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を適宜選択して用いることも可能となる。また、ICチップ近傍での弾性率を下げることで、異方性導電層の一例である封止シート材料のなかでの応力集中が緩和される。基板4に用いられる材料がセラミックのように固い(弾性率の高い)場合には、このような構造をとると、基板近傍での封止シート材料との弾性率、線膨張係数がマッチングして、尚、好適である。

【0141】一方、無機フィラー6fの少ない部分700又は樹脂層6xを基板側に配置した場合には、又は、基板側において無機フィラーフ分布を小さくした場合には、樹脂基板やフレキシブル基板(FPC)などのように基板4に曲げが加わるような場合において、基板4を電子機器の筐体に組み込む際に曲げ応力が加わるようなとき、基板4と異方性導電層の一例である封止シートとの密着強度を向上する目的で用いることができる。ICチップ側の表面層がポリイミド膜で形成された保護膜よりなる場合においては、一般に、絶縁性樹脂の密着が良好で、問題とならない場合にICチップ1から基板4にかけて、弾性率と線膨張係数が連続的または段階的に変化することで、ICチップ側で封止シートが固く、基板側では柔らかい材料とすることができる。これにより、封止シート内部での応力発生が小さくなることから信頼

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性が向上する。

【0142】さらに、ICチップ側と基板側の両側に無機フィラー6fの少ない部分700又は樹脂層6x, 6zを配置した場合、又は、ICチップ側と基板側の両側において無機フィラーフ分布を小さくした場合には、上記ICチップ側と基板側との2つの場合を両立させるものであり、ICチップ側及び基板側の両方での密着性を向上させることができるとともに、線膨張係数を下げてICチップ1と基板4の両者を高い信頼性で接続させることができる。また、ICチップ側表面の材質及び基板材質に応じて、より密着性、樹脂塗り性の良好な絶縁性樹脂を選択して用いることができる。また、これらの無機フィラー6fの量の多い少ないの傾斜は自由に変えることができるので、無機フィラー6fの少ない部分又は層を極薄くしたりすることで、基板材料とのマッチングが可能である。

【0143】(第15実施形態) 次に、本発明の第15実施形態においては、上記第8～14実施形態及びそれらの変形例にかかる回路基板への電子部品例えはICチップの実装方法及び装置及び上記実装方法により上記ICチップが上記基板に実装された電子部品ユニット若しくはモジュール例えは半導体装置により使用される異方性導電層の製造工程を図34、図35に基づいて説明する。

【0144】まず、直接、回路基板4上で異方性導電層を形成する場合には、回路基板4の上に、第1樹脂シートを貼付け、その上に第2樹脂シートを貼付ける。このとき、第1樹脂シートに無機フィラー6fが多い場合は図28(A)または図30のようになり、逆の場合には図28(B)または図31のようになる。すなわち、前者の場合には、第1樹脂シートは上記無機フィラー6fが多い部分701又は第2樹脂層6yに対応する樹脂シートであり、後者の場合には、上記無機フィラー6fが少ない部分700又は第1樹脂層6xに対応する樹脂シートとなる。

【0145】また、第2樹脂シートの上にさらに第3樹脂シートを形成して、第1樹脂シートと第3樹脂シートとが無機フィラー6fが少ない部分700又は第1樹脂層6xに対応する場合には、図28(C)または図32(A)のようになる。

【0146】また、これらを、図34、図35に示すように、予めセパレータと呼ばれるベースフィルム672上で、第1樹脂シート673と第2樹脂シート674とをこの順に(図34、図35にはこの場合のみ示す)、又はこれとは逆に、又はさらに第3樹脂シートをも、貼り付けて形成してもよい。この場合には、図34、図35のよう、上下一対の加熱可能なローラ670, 270などで複数の樹脂シート673, 674を、必要に応じて加熱しつつ、貼り付けていく。その後、形成された樹脂シート体671を所定寸法毎に切断す

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ば、図28(A)～(C)、図29(A)～(C)、図30～32のいずれかに示すような上記異方性導電膜シート10となる。

【0147】また、別の変形例として、異方性導電膜シート10が連続した異方性導電膜シート体を作製する際には、溶剤に溶かせたエポキシ及び無機フィラーをドクターブレード法などによりセパレーターと呼ばれるベースフィルム上に塗布する。この溶剤を乾燥させて異方性導電膜シート体が製作される。

【0148】このとき、一旦、無機フィラー6fの濃度が低いか、又は、無機フィラー6fが入っていない液体状の絶縁性樹脂を第1層としてベースフィルム上に塗布し、場合によっては、その塗布された第1層の乾燥を行う。乾燥しない場合には、無機フィラー6fが、若干、第1層に第2層の無機フィラー6fが混入していき、図33のように無機フィラー分布が傾斜した構造となる。

【0149】上記塗布形成された第1層の上に、無機フィラー6fを第1層よりも多く混入した液体状の絶縁性樹脂を塗布して第2層とする。第2層を乾燥することにより、ベースフィルム上に第1層と第2層とが形成された2層構造の異方性導電膜シート体が形成できる。異方性導電膜シート体を所定寸法毎に切断すれば、図28(A)、図29(A)、図30に示すような上記異方性導電膜シート10となる。

【0150】なお、基板側に無機フィラー6fが少ない層を配置する場合には、上記と逆の工程、すなわち、ベースフィルム上に第2層を形成したのち、第2層上に第1層を形成して、2層構造の異方性導電膜シート体が形成できる。異方性導電膜シート体を所定寸法毎に切断すれば、図28(B)、図29(B)、図31に示すような上記異方性導電膜シート10となる。

【0151】また、一旦、無機フィラー6fの濃度が低い、又は、無機フィラー6fが入っていない絶縁性樹脂6mを第1層として塗布乾燥（省略されることもある。）し、第1層の上に無機フィラー3fを第1層よりも多く混入した絶縁性樹脂を塗布して第2層として塗布乾燥（省略されることもある。）し、この上に無機フィラーの量が第2層より少ないまたは無い第3層を塗布する。これを乾燥することにより、ベースフィルム上に第1層と第2層と第3層とが形成された3層構造の異方性導電膜シート体が形成できる。異方性導電膜シート体を所定寸法毎に切断すれば、図28(C)、図29(C)、図32(A)に示すような上記異方性導電膜シート10となる。

【0152】上記直接、回路基板4上で異方性導電層を形成する方法によれば、上記電子部品ユニットを製造する側で、上記異方性導電層において、電子部品に最適な材料の樹脂を選択して電子部品側に配置する一方、基板に最適な材料の樹脂を選択して基板側に配置することができ、樹脂の選択の自由度を高めることができる。

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【0153】これに対して、異方性導電膜シート体を製造する方法では、上記したほど選択の自由度は無いが、一括して多数の上記異方性導電膜シート10を製造することができて、製造効率が良いとともに安価なものとなるとともに、貼り付け装置が1台で十分になる。

【0154】上記したように、本発明の上記各実施形態によれば、電子部品例えばICチップと回路基板を接合するのに従来要した工程の多くのを無くすことができ、非常に生産性を向上させることができる。すなわち、例え
10 ば、従来例として記載したスタッド・バンプ・ボンディングや半田バンプによる接合では、フリップチップ接合した後に封止材を注入してバッチ炉に入れて硬化する必要がある。この封止材の注入には、1ヶあたり数分、また、封止材の硬化に、2から5時間を要する。スタッド・バンプ・ボンディング実装においては、さらにその前行程として、バンプにAgペーストを転写して、これを基板に搭載した後、Agペーストを硬化するという工程が必要となる。この工程には2時間要する。これに対して、上記実施形態の方法では、上記封止工程を無くす
20 ことができる、非常に生産性を向上させることができる。さらに、上記実施形態では、固体又は半固体の絶縁性樹脂の封止シート等を用いることにより、例えば分子量の大きなエポキシ樹脂を用いることができることとなり、10～20秒程度の短時間で接合が可能となり、接合時間の短縮も図ることができ、さらに生産性を向上させることができる。さらに、以下のような効果をも奏することができる。

【0155】(1) バンプ形成

バンプをメッキで形成する方法（従来例3）では、専用のバンプ形成工程を半導体メーカーで行う必要があり、限定されたメーカーでしかバンプの形成ができない。ところが、本発明の上記実施形態によれば、ワイヤボンディング装置により、汎用のワイヤボンディング用のICチップを用いることができ、ICチップの入手が容易となる。すなわち、汎用のワイヤボンディング用のICチップを用いることができる理由は、ワイヤボンディングであれば、Alパッドが形成された通常のICパッド上に、ワイヤボンディング装置やバンプボンディング装置を用いてバンプが形成可能であるからである。一方、バンプをメッキで形成する方法（従来例3）によりメッキバンプを形成するには、Alパッドの上に、Ti、Cu、Crなどのバリヤメタルを形成したのちにレジストをスピンドルで塗布し、露光してバンプ形成部のみ穴を開ける。これに電気を通電して、その穴部分にAuなどからなるメッキを行うことで形成する。従って、メッキバンプを形成するには、大規模なメッキ装置や、シアノ化合物などの危険物の廃液処理装置を必要とするので、通常のアセンブリ工程を行う工場では現実には実施不可能である。

【0156】また、従来例1の方法に比べて、導電性接

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着剤の転写といった不安定な転写工程での接着剤の転写量を安定させるためのバンプレベリングが不要となり、そのようなレベリング工程用のレベリング装置が不要となる。その理由は、バンプを押圧しながら基板の電極上で押しつぶすため、予めバンプだけをレベリングしておく必要がないためである。

【0157】また、上記実施形態において以下のようにすれば、バンプ103を回路基板4の電極5にズレて実装された場合においても、信頼性の高い接合を達成することもできる。すなわち、バンプ3をICチップ1上に形成する際にワイヤボンディングと同様に金線を電気スパークにより金ボール96aを形成する。次に、95aで示す直径Φd-Bumpのボール96aを形成し、これをチャムファ一角θcが100°以下となるキャピラリー193の93aで示すチャムファ一直径ΦDを金ボール96aの直径d-Bumpの1/2から3/4とし、キャピラリー193の金ボール96aと接する部分に平らな部位を設けない先端形状としたキャピラリー193でICチップ1の電極2に超音波及び熱圧着によりバンプ103を形成する。上記形状のキャピラリー193を用いることで図10(B)のような先端が大略円錐状のバンプ103をICチップ1の電極2に形成することができる。上記方法で形成したバンプ103を回路基板4の電極5に図11(C)のごとく寸法Zだけズレて実装された場合においても、バンプ103がその先端が大略円錐形であるためバンプ103の外径の半分までのズレである場合はバンプ103の一部が必ず基板4の電極5と接触することができる。従来のバンプ3の図11(D)ではバンプ3のいわゆる台座3gの幅寸法dの一部が接触するが、部分的にしか接触せず不安定な接合となる。これを冷熱衝撃試験やリフローにかけた場合に接合部分がオーブンとなる。本発明では、このような不安定な接合がなくなり、生産歩留まりと信頼性の高い接合を提供することができる。

【0158】(2) ICチップと回路基板の接合
従来例2の方法によれば、接続抵抗は、バンプと回路基板の電極の間に存在する導電粒子の数に依存していたが、本発明の上記実施形態では、ICチップ側電極と基板側電極との間の電気的導通のために導電粒子を両電極間に挟み込む必要が無く、独立した工程としてのレベリング工程においてバンプ3をレベリングせずに回路基板4の電極5に従来例1、2よりも強い荷重(例えば、1バンプ3あたり20gf以上の加圧力)で押しつけてバンプ3と電極5とを直接的に接合することができるため、介在する粒子数に接続抵抗値が依存せず、安定して接続抵抗値が得られる。すなわち、上記導電粒子10aは、バンプ3と基板電極5との直接接合において、導電粒子10aがバンプ3と基板電極5との間に挟まれた場合には、基板側の電極5とICチップ側のバンプ3との間での接続抵抗値を低下せしめることができるといつ

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た、付加的効果を奏するものである。

【0159】また、従来のレベリング工程では基板電極との接合時のバンプ高さを一定に整えるために行っているが、本発明の上記各実施形態ではバンプ3の押しつぶしを電極2又は5への接合と同時に行うことができるので、独立したレベリング工程が不要であるばかりでなく、接合時に回路基板4の反りやうねりを変形させて矯正しながら接合することができるので、又は、バンプ3, 103に付着させた導電性ペーストを硬化して接合時に導電性ペーストを変形させることにより、バンプ3, 103のレベリングを一切不要として、接合時に回路基板4の反りやうねりを変形させて矯正しながら接合するので、反りやうねりに強い。

【0160】ところで、従来例1では10μm/ICチップ(1個のICチップ当たり10μmの厚み反り寸法精度が必要であることを意味する。)、従来例2では2μm/IC、従来例3でも1μm/ICチップ(バンプ高さバラツキ±1μm以下)というような高精度の基板4やバンプ3, 103の均一化が必要であり、実際にLCDに代表されるガラス基板が用いられている。これに対して、本発明の上記実施形態によれば、接合時に回路基板4の反りやうねりを変形させて矯正しながら接合するので、反りやうねりのある平面度の悪い基板、例えば、樹脂基板、フレキシブル基板、多層セラミック基板などを用いることができ、より低廉で汎用性のあるICチップの接合方法を提供することができる。

【0161】また、ICチップ1と回路基板4との間の熱硬化性樹脂6mの体積をICチップ1と回路基板4との間の空間の体積より大きくするようにすれば、この空間からはみ出すように流れ出て、封止効果を奏することができる。よって、従来例1で必要とした導電性接着剤でICチップと回路基板を接合した後にICチップの下に封止樹脂(アンダーフィルコート)を行う必要がなく、工程を短縮することができる。

【0162】なお、無機フィラー6fを熱硬化性樹脂6mにその5~90wt%程度配合することにより、熱硬化性樹脂の弾性率、熱膨張係数を基板4に最適なものにコントロールすることができる。これに加えて、通常のメッキバンプでこれを利用すると、バンプと回路基板の間に無機フィラーが入り込み、接合信頼性が低くなる。しかしながら、本発明の上記実施形態のようにスタッドバンプ(ワイヤーボンディングを応用した形成方法)を用いるようにすれば、接合開始当初に熱硬化性樹脂6m中に入り込んできた尖っているバンプ3, 103により、無機フィラー6fを、よって、熱硬化性樹脂6mを、バンプ3, 103の外側方向へ押し出さすことにより、バンプ3, 103が変形していく過程で無機フィラー6fと熱硬化性樹脂6mをバンプ3, 103と電極5, 2の間から押し出し、不要な介在物を存在させないようにすることができ、より信頼性を向上させることができ

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できる。

【0163】以上、本発明によれば、従来の接合工法よりも生産性よく、低廉な電子部品例えばICチップと回路基板の接合方法及びその装置を提供することができる。

【0164】なお、上記第1実施形態においては、レベリングをしない図1に示すようなバンプ3の他、図37(A), (B)にそれぞれ示すようなレベリング済みのスタッドバンプ300, 301を有するICチップ1と基板4との間での接合にも適用することができる。この場合、レベリング工程は必要となるが、封止工程が不要となるなどの他の効果は奏すことができる。また、上記バンプは、めっき又は印刷により、外観が図37

(A), (B)と大略同様に形成されたバンプを使用することもできる。例えば、ICチップの電極上にチタンやニッケルや金をこの順にめっきでバンプを形成したり、アルミニウムやニッケルなどと合成樹脂とを混合したペーストをICチップの電極上に印刷して乾燥又は硬化させることにより、ポリマーバンプを形成することもできる。特に、レベリングしたバンプやめっき又は印刷により形成したバンプを使用する場合、バンプの変形量を少ないため、万が一、無機フィラーがバンプと基板電極との間に挟まれてしまってバンプと基板電極との間の電気的接続が不安定になる恐れがあるが、バンプと基板電極との間に導電粒子10aも挟まれることになり、この導電粒子10aによりバンプと基板電極との間の導通を確保することができる。

【0165】

【発明の効果】上記したように、本発明によれば、電子部品と回路基板を接合するのに従来要した工程の多くを無くすことができ、非常に生産性を向上させることができる。

【0166】さらに、以下のような効果をも奏することができる。

【0167】(1) バンプ形成

バンプをメッキで形成する方法(従来例3)では、専用のバンプ形成工程を半導体メーカーで行う必要があり、限定されたメーカーでしかバンプの形成ができない。ところが、本発明によれば、ワイヤボンディング装置により、電子部品の例として汎用のワイヤボンディング用のICチップを用いることができ、ICチップの入手が容易となる。

【0168】また、従来例1の方法に比べて、導電性接着剤の転写といった不安定な転写工程での接着剤の転写量を安定させるためのバンプレベリングが不要となり、そのようなレベリング工程用のレベリング装置が不要となる。

【0169】また、先端が大略円錐状のバンプを電子部品の電極に形成すれば、バンプを回路基板の電極にズレて実装された場合においても、バンプがその先端が大略

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円錐形であるためバンプの外径の半分までのズレである場合はバンプの一部が必ず基板の電極と接触することができる。従来のバンプではバンプのいわゆる台座の一部が接触するが、部分的にしか接触せず不安定な接合となる。これを冷熱衝撃試験やリフローにかけた場合に接合部分がオープンとなる。本発明では、このような不安定な接合がなくなり、生産歩留まりと信頼性の高い接合を提供することができる。

【0170】(2) ICチップと回路基板の接合

従来例2の方法によれば、接続抵抗は、バンプと回路基板の電極の間に存在する導電粒子の数に依存していたが、本発明では、電子部品側電極と基板側電極との間の電気的導通のために導電粒子を両電極間に挟み込む必要が無く、独立した工程としてのレベリング工程においてバンプをレベリングせずに回路基板の電極に従来例1、2よりも強い荷重(例えば、1バンプあたり20g以上上の加圧力)で押しつけてバンプと電極とを直接的に接合することができるため、介在する粒子数に接続抵抗値が依存せず、安定して接続抵抗値が得られる。すなわち、上記導電粒子は、バンプと基板電極との直接接合において、導電粒子がバンプと基板電極との間に挟まれた場合には、基板側の電極と電子部品側のバンプとの間での接続抵抗値を低下せしめることができるといった、附加的効果を奏するものである。

【0171】また、従来のレベリング工程では基板電極との接合時のバンプ高さを一定に整えるために行っているが、本発明ではバンプの押しつぶしを電極への接合と同時に行うことができるので、独立したレベリング工程が不要であるばかりでなく、接合時に回路基板の反りやうねりを変形させて矯正しながら接合することができるので、又は、バンプに付着させた導電性ペーストを硬化して接合時に導電性ペーストを変形させることにより、バンプのレベリングを一切不要として、接合時に回路基板の反りやうねりを変形させて矯正しながら接合するので、反りやうねりに強い。

【0172】ところで、従来例1では10μm/ICチップ(1個のICチップ当たり10μmの厚み反り寸法精度が必要であることを意味する)、従来例2では2μm/IC、従来例3でも1μm/ICチップ(バンプ高さバラツキ±1μm以下)というような高精度の基板やバンプの均一化が必要であり、実際には、LCDに代表されるガラス基板が用いられている。これに対して、本発明によれば、接合時に回路基板の反りやうねりを変形させて矯正しながら接合することができるので、反りやうねりのある平面度の悪い基板、例えば、樹脂基板、フレキシブル基板、多層セラミック基板などを用いることができ、より低廉で汎用性のあるICチップの接合方法を提供することができる。

【0173】また、電子部品と回路基板との間の絶縁性樹脂の体積を電子部品と回路基板との間の空間の体積よ

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り大きくするようすれば、この空間からはみ出すように流れ出て、封止効果を奏すことができる。よって、従来例1で必要とした導電性接着剤でICチップと回路基板を接合した後にICチップの下に封止樹脂（アンダーフィルコート）を行う必要がなく、工程を短縮することができる。

【0174】なお、無機フィラーを絶縁性樹脂にその5～90wt%程度配合することにより、絶縁性樹脂の弾性率、熱膨張係数を基板に最適なものにコントロールすることができる。これに加えて、通常のメッキバンプでこれを利用すると、バンプと回路基板の間に無機フィラーが入り込み、接合信頼性が低くなる。しかしながら、本発明のようにスタッドバンプ（ワイヤーボンディングを応用した形成方法）を用いるようにすれば、接合開始当初に絶縁性樹脂中に入り込んできた尖っているバンプにより、無機フィラーを、よって、絶縁性樹脂を、バンプの外側方向へ押し出すことにより、バンプが変形していく過程で無機フィラーと絶縁性樹脂をバンプと電極の間から押し出し、不要な介在物を存在させないようにすることができ、より信頼性を向上させることができる。

【0175】また、同じ重量の無機フィラーを配合する場合には、平均粒径が3μm以上の大きな無機フィラーを用いるようにするか、複数の異なる平均粒径を持つ無機フィラーを用いるようにするか、一方の無機フィラーの平均粒径は、他方の無機フィラーの平均粒径の2倍以上異なっている無機フィラーを用いるようにするか、少なくとも2種類の無機フィラーのうちの一方の無機フィラーは3μmを超える平均粒径を持ち、他方の無機フィラーは3μm以下の平均粒径を持つ無機フィラーを用いるようにすれば、無機フィラーの周りにおける吸湿量を減らしめることができ、耐湿性を向上させることができるとともに、無機フィラーの量を増加させることができて、フィルム化（固体化）することが容易になる上に、異方性導電層例えば異方性導電膜シート又は異方性導電膜形成用接着剤の線膨張係数を低下させることができ、より長寿命化させてることができ、信頼性を向上させることができる。

【0176】さらに、平均粒径の大きい一方の無機フィラーは上記絶縁性樹脂と同一材料からなるようにすれば、応力緩和作用を奏するようにすることができ、又、平均粒径の大きい一方の無機フィラーは上記絶縁性樹脂であるエポキシ樹脂よりも柔らかく、上記一方の無機フィラーが圧縮されるようすれば、応力緩和作用を奏するようにすることができる。

【0177】また、電子部品又は上記基板と異方性導電層との接合界面では無機フィラーが存在しないかその量を少なくすれば、絶縁性樹脂本来の接着性が発揮されて、上記接合界面で接着性の高い絶縁性樹脂が多くなり、電子部品又は上記基板と絶縁性樹脂との密着強度を

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向上させることができて、無機フィラーによる線膨張係数を下げる効果を持たせたまま、電子部品又は上記基板との接着性が向上する。これにより、各種信頼性試験での寿命が向上するとともに、曲げに対しての剥離強度が向上する。

【0178】さらに、上記電子部品に接触する部分又は層では、電子部品表面に用いられる膜素材に対して密着性を向上させる絶縁性樹脂を用いる一方、上記基板に接觸する部分又は層では、基板表面の材料に対して密着性を向上させる絶縁性樹脂を用いるようすれば、さらに密着性を向上させることができる。なお、上記各実施形態において、上記超音波を印加して上記金バンプと上記基板の上記電極とを金属接合するとき及び上記基板の反りの矯正と上記バンプを押しつぶすときの両方の工程において上記電子部品及び基板の両方とも加熱することなく、それぞれ、行ったのち、上記電子部品側から、又は基板側から、又は、上記電子部品側と上記基板側の両方から加熱するようにしてもよい。

【0179】以上、本発明によれば、回路基板と電子部品を接合した後に、電子部品と基板の間に流し込む封止樹脂工程やバンプの高さを一定に揃えるバンプレベリング工程を必要とせず、電子部品を基板に生産性良くかつ高信頼性で接合する回路基板への電子部品の実装方法及び装置を提供することができる。

【図面の簡単な説明】

【図1】 (A)、(B)、(C)、(D)、(E)、(F)、(G)はそれぞれ本発明の第1実施形態にかかる回路基板への電子部品例えはICチップの実装方法を示す説明図である。

【図2】 (A)、(B)はそれぞれ第1実施形態にかかる回路基板への電子部品例えはICチップの実装方法において、熱硬化性樹脂中の無機フィラーが接合開始当初に熱硬化性樹脂中に入り込んできた尖っているバンプによりバンプ外側方向へ押し出される状態を示す説明図、及び、(C)はバンプと基板電極の間に無機フィラーが入り込まない状態を示す説明図である。

【図3】 (A)、(B)、(C)、(D)、(E)、(F)、(G)はそれぞれ本発明の第1実施形態における実装方法において、ICチップのワイヤボンダーを用いたバンプ形成工程を示す説明図である。

【図4】 (A)、(B)、(C)はそれぞれ本発明の第1実施形態にかかる実装方法において、回路基板とICチップの接合工程を示す説明図である。

【図5】 (A)、(B)、(C)はそれぞれ本発明の第1実施形態である実装方法において回路基板とICチップの接合工程を示す説明図である。

【図6】 (A)、(B)、(C)は、それぞれ、本発明の第3実施形態の実装方法において異方性導電膜シートに代えて、熱硬化性接着剤を回路基板上に配置することを説明するための説明図、及び、(D)、(E)はそ

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れぞれ上記第1実施形態での接合状態の拡大説明図である。

【図7】 (A)、(B)、(C)、(D)、(E)、(F)は、それぞれ、本発明の第3実施形態の実装方法において、図6の変形例として、異方性導電膜シートに代えて、熱硬化性接着剤を回路基板上に配置することを説明するための説明図である。

【図8】 (A)、(B)、(C)はそれぞれ本発明の第5実施形態にかかる実装方法において、回路基板とICチップの接合工程を示す説明図である。

【図9】 (A)、(B)、(C)はそれぞれ本発明の第5実施形態である実装方法において回路基板とICチップの接合工程を示す説明図である。

【図10】 (A)、(B)、(C)、(D)はそれぞれ本発明の第6実施形態である実装方法において回路基板とICチップの接合工程を示す説明図である。

【図11】 (A)、(B)、(C)、(D)、(E)はそれぞれ本発明の第6実施形態である実装方法において回路基板とICチップの接合工程を示す説明図である。

【図12】 (A)、(B)、(C)、(D)はそれぞれ本発明の第7実施形態である実装方法において回路基板とICチップの接合工程を示す説明図である。

【図13】 は本発明の第7実施形態である実装方法において回路基板とICチップの接合工程を示す説明図である。

【図14】 (A)、(B)はそれぞれ熱硬化性樹脂シートをICチップ1側に形成した第1実施形態の変形例を示す説明図、及び、熱硬化性接着剤をICチップ1側に形成した第1実施形態の変形例を示す説明図である。

【図15】 従来の回路基板とのICチップの接合方法を示す断面図である。

【図16】 (A)、(B)はそれぞれ従来の回路基板とのICチップの接合方法を示す説明図である。

【図17】 上記第1実施形態において、 $80\mu m$ の外径のバンプの場合の抵抗値と荷重との関係のグラフの図である。

【図18】 上記第1実施形態において、 $80\mu m$ 、 $40\mu m$ のそれぞれの外径のバンプと最低荷重との関係に基づき信頼性の高い領域を示したグラフの図である。

【図19】 上記第3実施形態において、樹脂シート(異方性導電膜シート)の加熱温度と反応率とのグラフの図である。

【図20】 上記第1実施形態で使用される電子部品搭載装置の斜視図である。

【図21】 (A)、(B)、(C)、(D)はそれぞれ図20の電子部品搭載装置での部品側での位置認識動作を示す斜視図、部品の位置認識画像の図、基板側での位置認識動作を示す斜視図、基板の位置認識画像の図である。

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【図22】 上記第4実施形態で使用する超音波印加装置の概略図である。

【図23】 上記第5実施形態で使用される貼り付け装置の概略図である。

【図24】 (A)、(B)はそれぞれACF工法と上記実施形態の工法との比較説明のためのバンプ付近の拡大断面図である。

【図25】 本発明の第9実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により接合された接合状態の模式断面図である。

【図26】 上記第9実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される樹脂シートの部分拡大模式断面図である。

【図27】 本発明の第13実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により接合された接合状態での絶縁性樹脂と無機フィラーの模式断面図である。

【図28】 (A)、(B)、(C)、(D)はそれぞれ本発明の第14実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層の種々の例を示す電子部品ユニットの模式断面図である。

【図29】 (A)、(B)、(C)、(D)はそれぞれ本発明の第14実施形態の変形例にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層の種々の例の模式断面図である。

【図30】 図29(A)に示された上記第14実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層を使用して接合された接合状態の模式断面図である。

【図31】 図29(B)に示された上記第14実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層を使用して接合された接合状態の模式断面図である。

【図32】 (A)、(B)は図29(C)、(D)にそれぞれ示された上記第14実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層を使用して接合された接合状態の模式断面図である。

【図33】 (A)、(B)、(C)、(D)、(E)、(F)はそれぞれ上記第14実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層の無機フィラーの量と異方性導電層の厚み方向の位置との様々な関係のグラフを示す図である。

【図34】 本発明の第15実施形態にかかる回路基板への電子部品例えればICチップの実装方法及び装置により使用される異方性導電層の製造工程の説明図である。

【図35】 図34の部分拡大図である。

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【図36】 上記第1実施形態の一具体例における導電粒子の平均直径と無機フィラーの粒子の平均直径の分布図である。

【図37】 (A), (B) はそれぞれ上記第1実施形態の変形例において使用可能なバンプの例を示す図である。

【符号の説明】

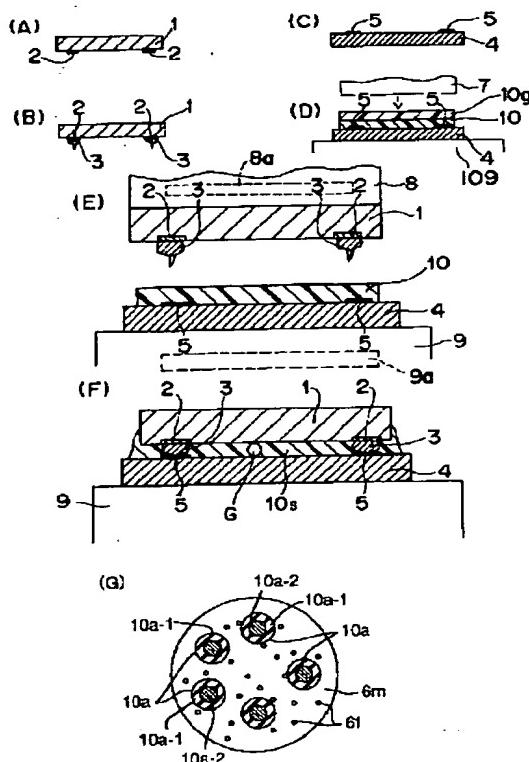
1…ICチップ、2…電極、3…103…バンプ、
3g…台座、4…回路基板、6b…異方性導電膜形成用
熱硬化性接着剤、6f…無機フィラー、6f-1…平均
粒径の大きな無機フィラー、6f-2…平均粒径の小
さな無機フィラー、6m…異方性導電層(例としては熱硬
化性樹脂)、6v…第4樹脂層、6w…第5樹脂層、6
x…第1樹脂層、6y…第2樹脂層、6z…第3樹脂
層、7…貼付けツール、8…接合ツール、8a…ヒー

(29)

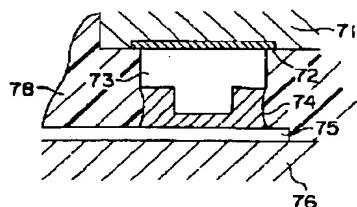
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タ、9、109、201…ステージ、10…異方性導電
膜シート、10a…導電粒子、10s…異方性導電膜シ
ートを構成していて硬化した樹脂、93、193…キャ
ピラリー、193a…先端部位、93b…平らな部位、
95…ワイヤ、96、96a…ボール、98…湾曲部、
99…ループ、200…保持部材、670…ローラ、6
71…絶縁性樹脂シート体、672…ベースフィルム、
673…第1樹脂シート、674…第2樹脂シート、7
00…ICチップ及び/又は基板に接触する部分(無機
フィラー量が少ない部分)、701…他の部分(無機フィラー量が
多い部分)、702…無機フィラー量が少ない部分、もしくは上記無機フィラーを配合しない部分、703…無機
フィラー量が多い部分。

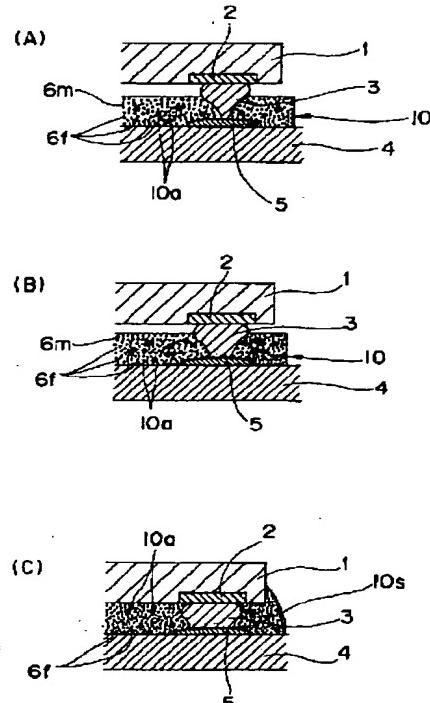
【図1】



【図15】

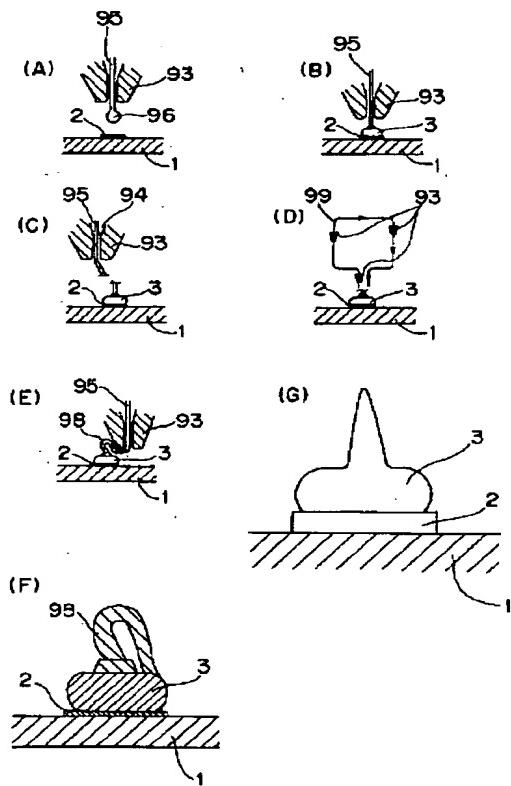


【図2】

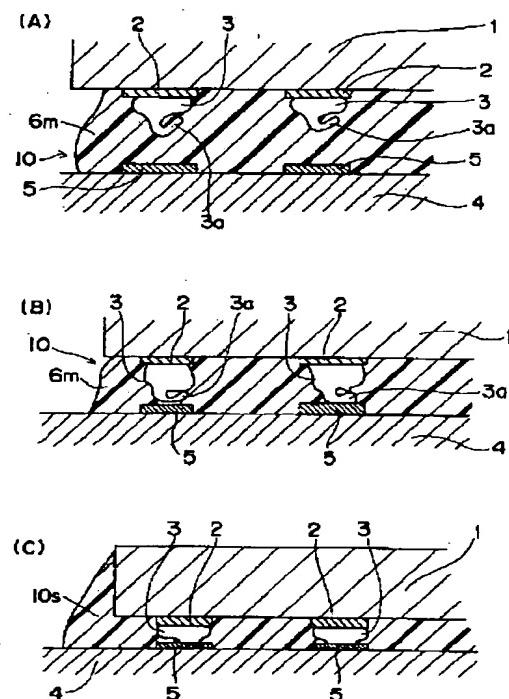


(30)

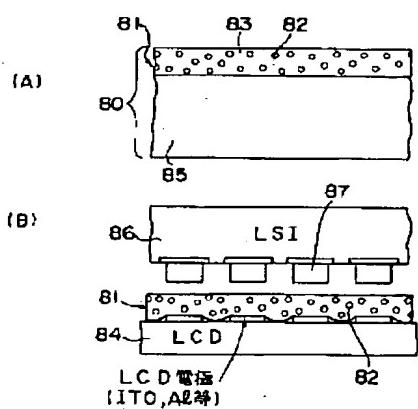
【図3】



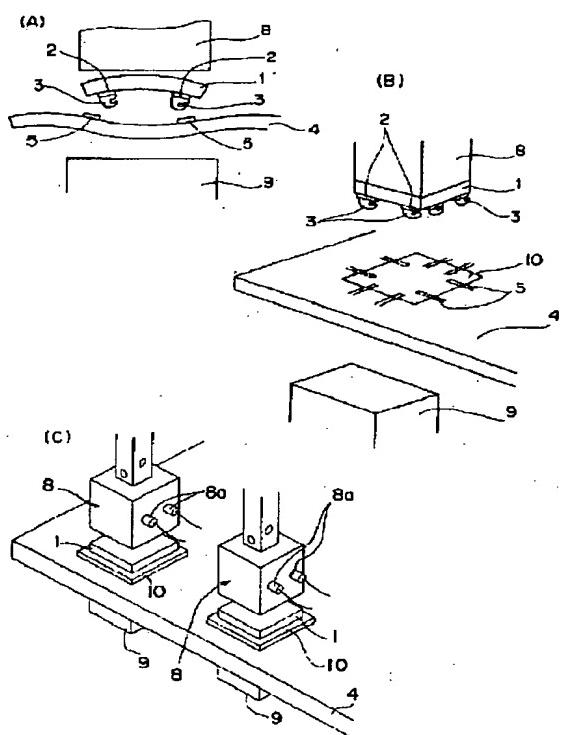
【図4】



【図16】

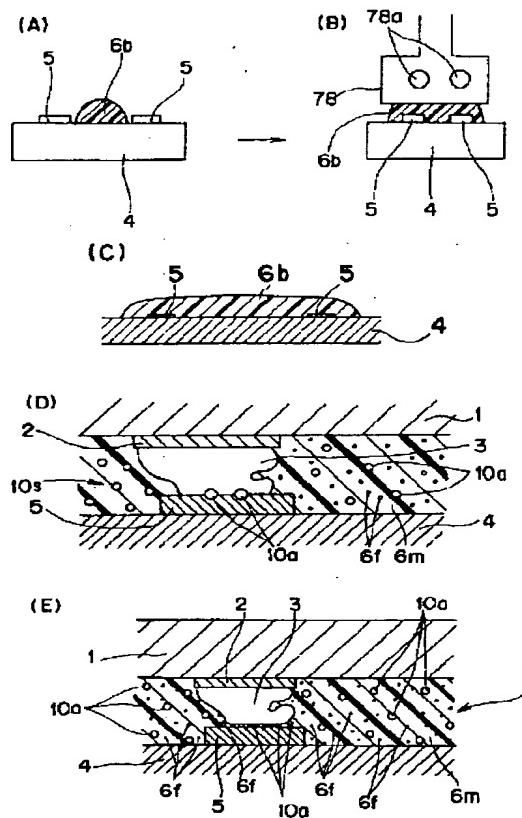


【図5】

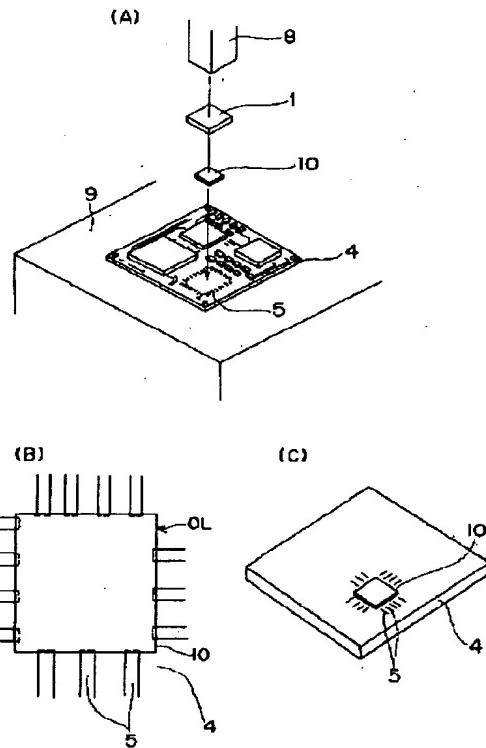


(31)

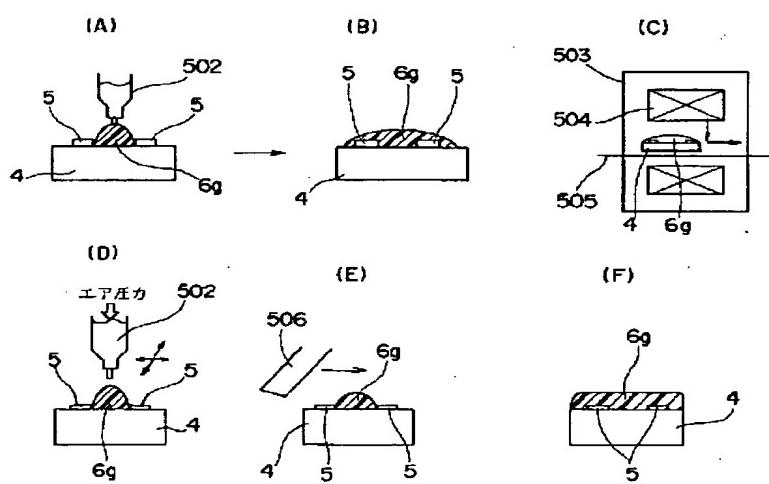
【図6】



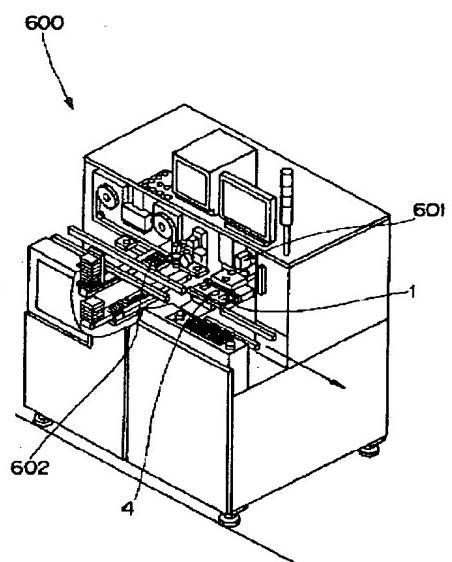
【図8】



【図7】

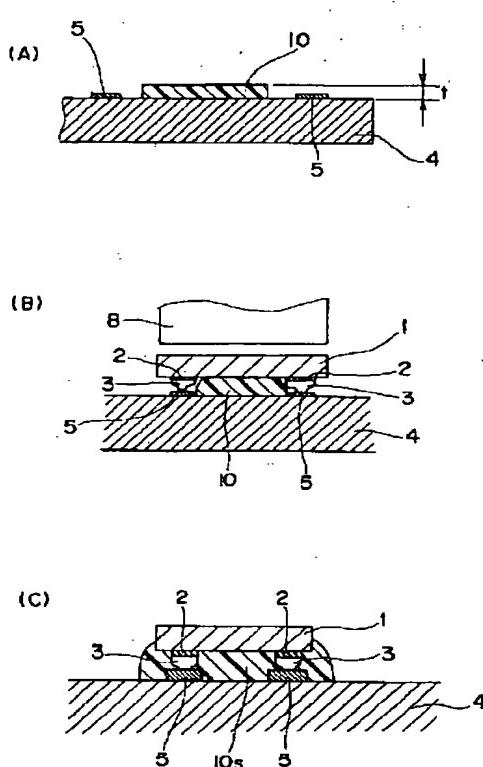


【図20】

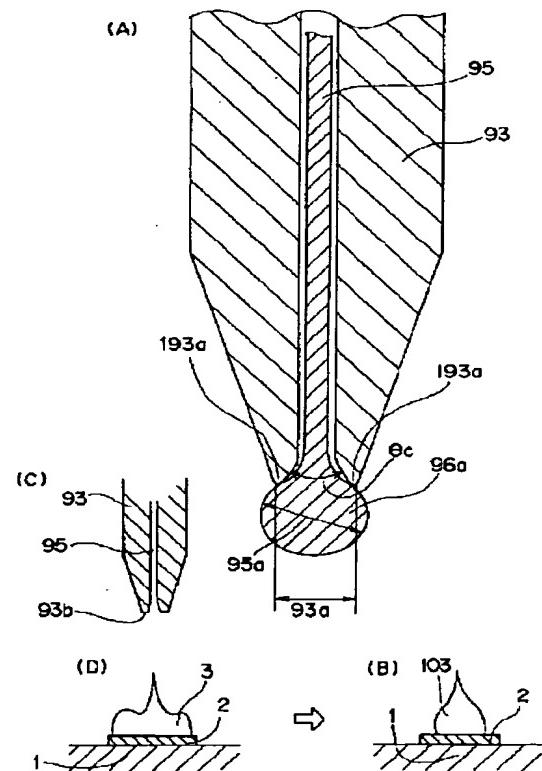


(32)

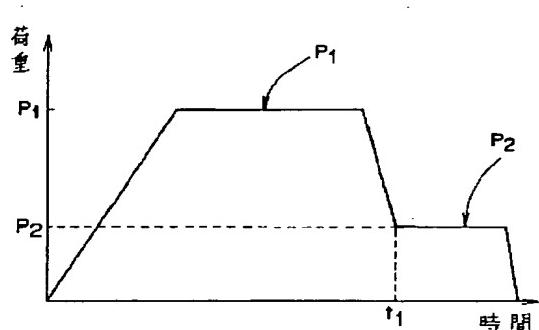
【図9】



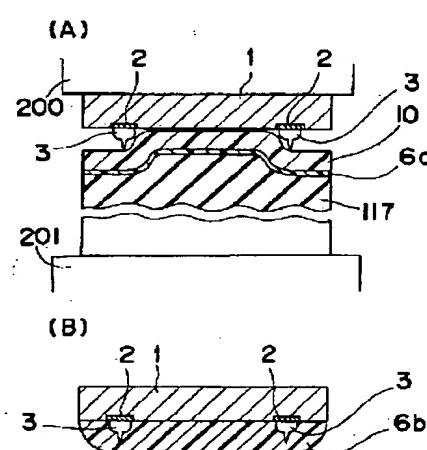
【図10】



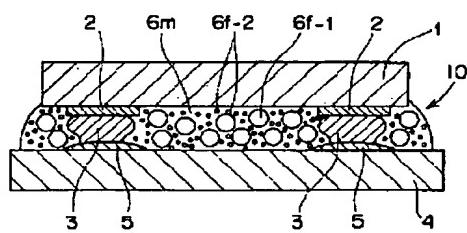
【図13】



【図14】

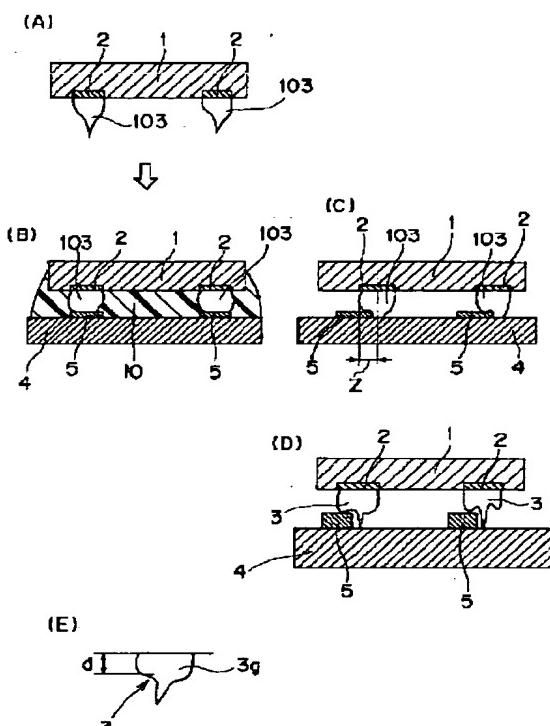


【図25】

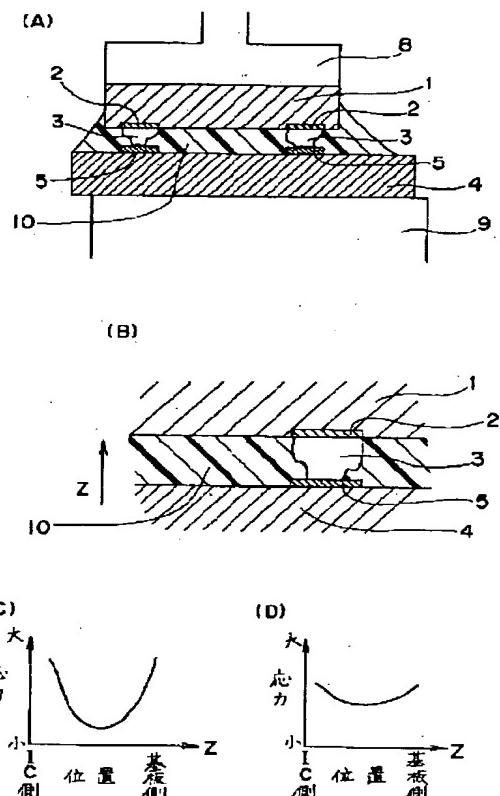


(33)

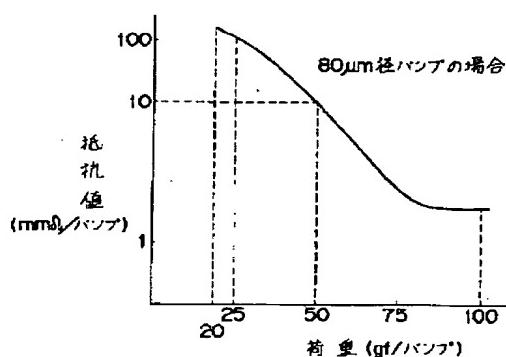
【図11】



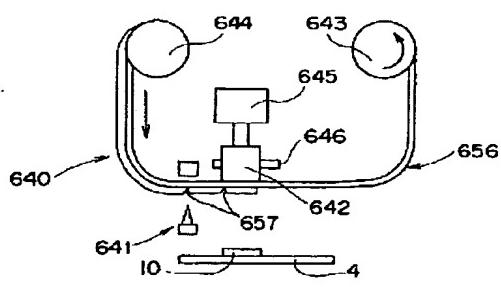
【図12】



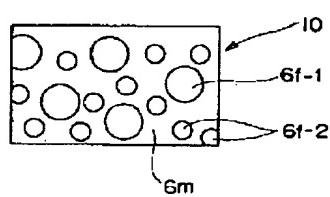
【図17】



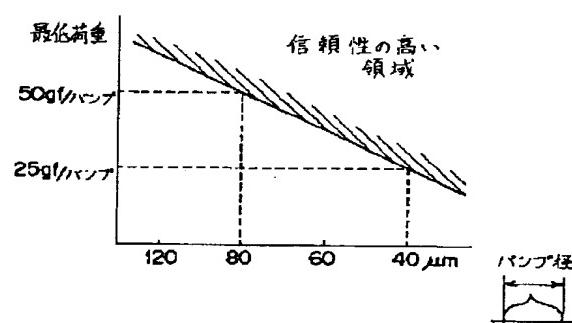
【図23】



【図26】

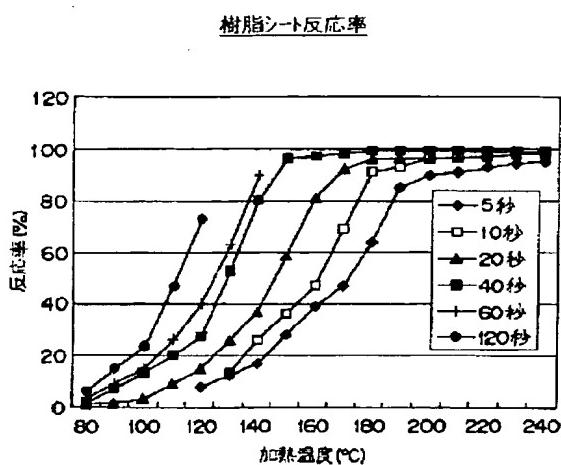


【図18】

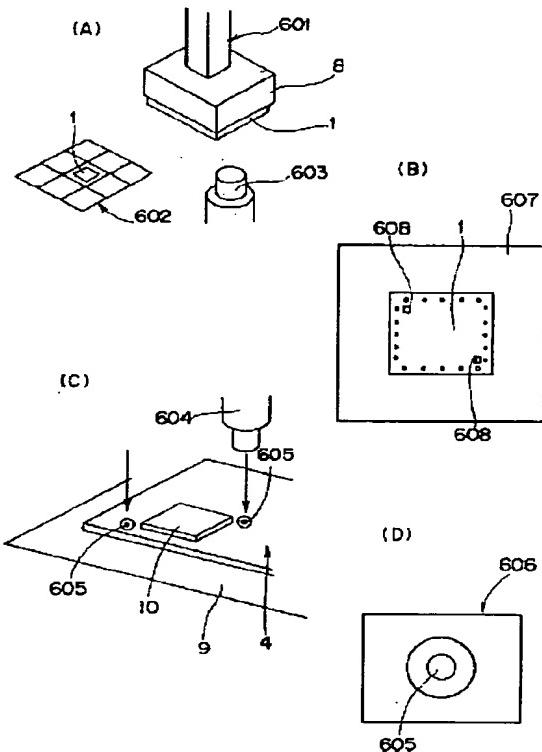


(34)

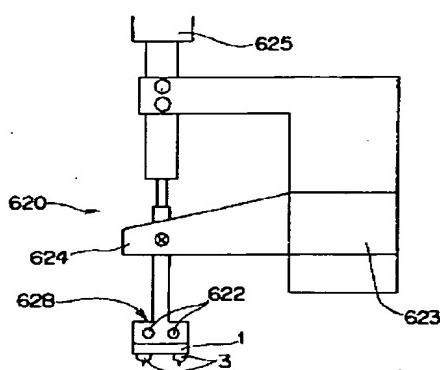
【図19】



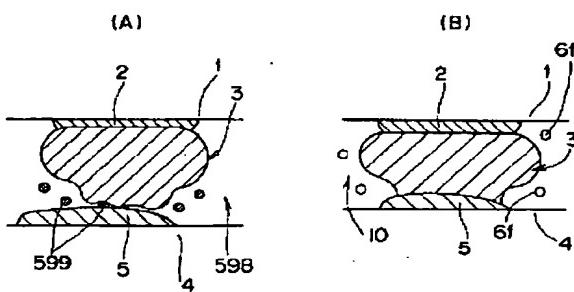
【図21】



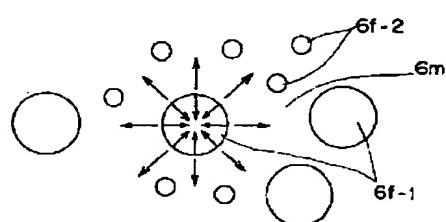
【図22】



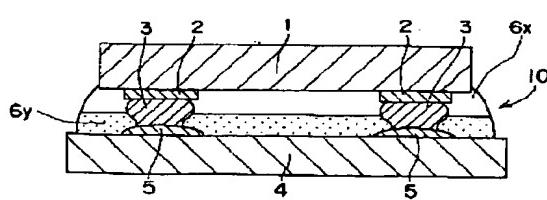
【図24】



【図27】

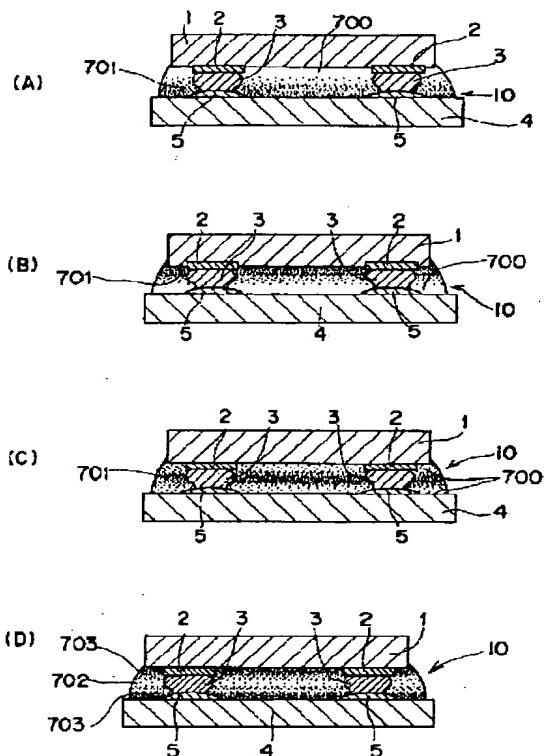


【図30】

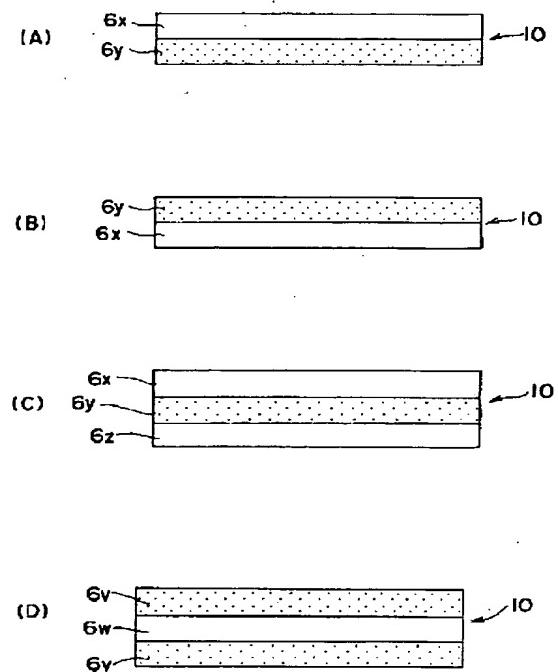


(35)

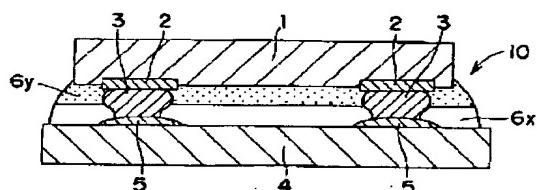
【図28】



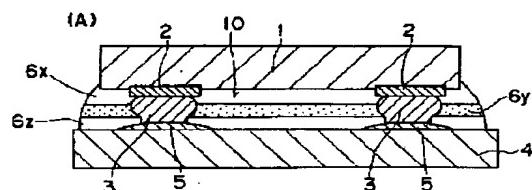
【図29】



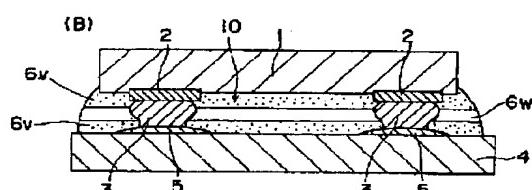
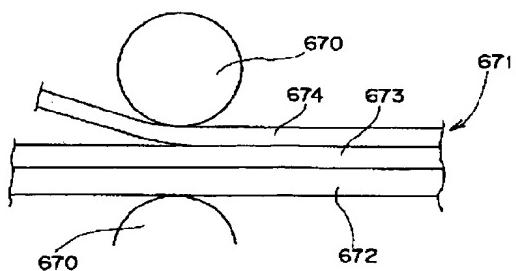
【図31】



【図32】

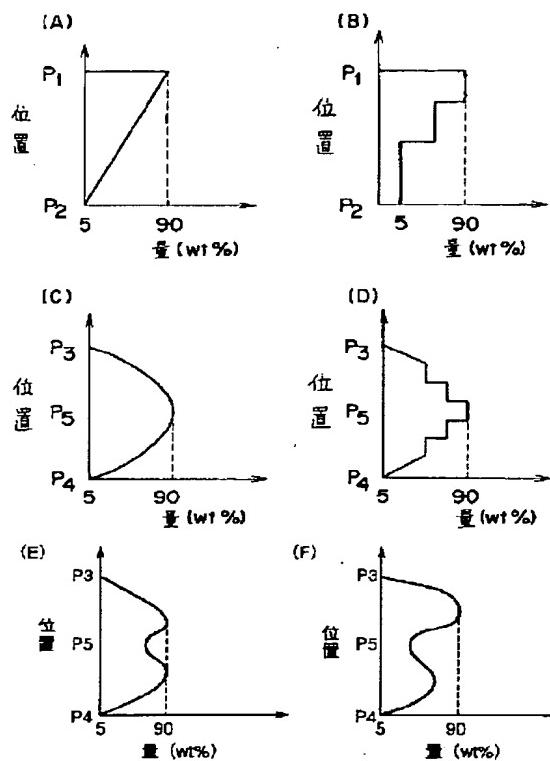


【図35】

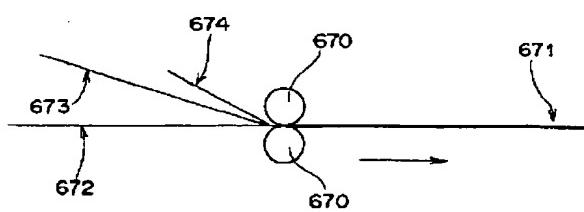


(36)

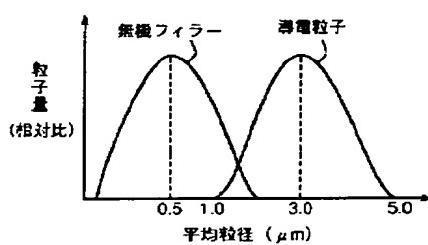
【図33】



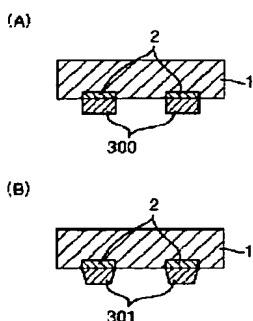
【図34】



【図36】



【図37】



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